

Effective Thermoelectric Performance in Silicon by Defect Engineering

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Abstract

Silicon offers many advantages as a next generation thermoelectric material, meeting modern demands for earth abundance and non-toxicity while demonstrating compatibility with large scale manufacturing. Highly doped silicon has a thermoelectric power factor equal to current commercial materials; however the efficiency with which it can convert power and the effectiveness with which it can maintain the temperature gradients required for this conversion are negatively impacted by high thermal conductivity. Addressing this challenge typifies modern silicon thermoelectric research. Solutions have been found at the nanoscale, but nano-material dimensions introduce new challenges around translation to devices. In this work, large concentrations of vacancy defects are introduced to thin-film single crystalline silicon (c-Si) up to $2\text{ }\mu\text{m}$ thick for the first time and shown to reduce room temperature thermal conductivity by 97%. Effects have no nanodependence and material is visually indistinguishable from defect free bulk. Improvements in thermoelectric performance are investigated using n-type and p-type materials and comparative evaluation reveals an increase over benchmark bulk c-Si by a factor of 14. Best results return a value of z comparable with best results of SiGe. The first time for such a value in c-Si at these device-applicable material thicknesses.

Dedication

This thesis is dedicated to my Family, my Wife and to my Children. Thank you all for your ever present horizon; and for your unending supplies of support, encouragement, and love. Without you not only would the finish line have remained distant, but the starting line would have never been possible.

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Samuel Johnson succinctly suggested that, “Few things are impossible to diligence and skill. Great works are performed not by strength, but by perseverance.” It is not too difficult to image a hushed voice somewhere amongst those gathered coolly adding, “..... and an army of help besides.”

This is most certainly true for this “great” work presented here. Without the support and time of so many this thesis would have remained out of reach no matter the lashings of perseverance and diligence applied.

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Chapter 1: Introduction

1.1 Introduction

The effective conversion of waste heat into electrical power remains a major challenge of modern times. Economic growth, Environmental sustainability and Energy access and security; the three cornerstones of the World Economic Forum's energy architecture performance index all present opportunities for improvement if the challenge of waste heat reutilisation can be tackled [1]. At a smaller scale, micro-harvesting of waste heat offers user-orientated opportunities rather than solutions to such global objectives. Nonetheless, interest is significant and impacts tangible. In an increasingly interconnected world, a developing range of consumer electronics, wearables, medical devices and real time communication devices all seek power solutions to secure improved utility and function. Harvesting waste heat and directly converting to electrical power at this micro scale offers one possibility, creating opportunity for extended battery life, trickle charging or direct operation.

Perhaps in part as a result of these emerging applications, the field of thermoelectric research has undergone resurgence in recent years. While interest during the 1950's and early 1960's was high, by 1965 research publications were in decline as major corporate interest waned [2]. Thermoelectric devices were resigned to a role of niche product, operating in aerospace and military applications where scalable, reliable power provision was a higher priority than efficiency [3]. The new generation of thermoelectric materials research can be summarised by two significant developments; the introduction of the nanoscale and significant increases in the potential conversion efficiency of new materials [4]. This combination has found figure-of-merit increasing by almost a factor of 3 as new materials are reported and traditional materials are reconsidered [5].

The introduction of nanoscale effects to thermoelectric material research builds on foundational work presented by Hicks and Dresselhaus in 1993 [6, 7]. The idea that the nanoscale could be used to generate freedom with which to control typically interdependent material properties was transformative. Not only could new materials now be designed but structures and meta-materials could be engineered to capitalise on predicted and reported effects.

The reporting of these effects on silicon nanowires in 2008 by Hochbaum et al [8] and Boukai et al [9] signalled the start of broad research efforts to produce thermoelectric materials from single crystal silicon (c-Si), offering potential access to a material with strong industrial links, abundance and low cost. The effect of phonon scattering as a result of small wire diameters and rough nanowire surfaces was found to reduce thermal conductivity significantly, increasing thermoelectric potential by two orders of magnitude. The development of nanowires from these initial studies on single wires to meta-materials such as complex nanowire forests [10] in less than a decade emphasises the rapid rate of innovation being undertaken.

As an area of fundamental research that is inherently application driven, future progress in thermoelectric materials must take care to ensure that solutions and applications do not decouple under such rapid development. Current commercial materials of bismuth telluride and lead telluride offer good performance but are poorly equipped to meet modern and emerging needs. The need for tomorrow's high performance material is one combining earth abundance with non-toxicity [11]. Consideration of process suitability must also be considered during design. While nanoscale features offer access to increasing thermoelectric potential, the commercial manufacture and application of often delicate structures can be expected to present challenges. Progress in materials such as interconnected nanowire arrays offer a view of what may be possible where research remains linked to concerns of application. These nanowire based materials demonstrated surface areas in the order of mm^2 capable of mitigating performance degradation resulting from random nanowire failure [12].

He & Tritt suggested that breakthroughs in multiscale defect engineering would, in part, hold the key to realising the next generation of materials [11]. The addition of extended defects to nanowires has been reported to increase Seebeck coefficient, with dislocation loops hypothesised to provide filtering of low energy charge carriers [13], while the introduction of point defects to c-Si nanofilms was reported to provide an almost 20 fold increase in thermoelectric figure-of-merit over that of bulk c-Si leaving manufactured material visually indistinguishable from control samples [14]. Such findings were in line with theoretical predictions reported by Lee et al, where NEMD simulations suggested c-Si thermal conductivity could be reduced by 95% through the introduction of vacancy defect concentrations at 1.5% [15].

This thesis reports on the application of defect engineering to c-Si material with thicknesses $> 1 \mu\text{m}$; demonstrating that reductions in thermal conductivity using a method of introduction reported by Bennett et al [14] can be successful on materials with thicknesses more than an order of magnitude greater. A modified approach is also developed and tested for the first time, removing any reliance on an isolating layer of buried oxide and demonstrating comparable reductions to thermal conductivity on free-standing thin-films. These thicknesses and materials offer practical utility to thin-film based thermoelectric devices suitable for microharvesting and provide a crucial step towards realisation of a next generation thermoelectric material.

1.2 Objectives

The main objectives of this work can be categorised under three headings:

1. ***Demonstration of upscaling of the vacancy defect engineering technique.*** While proof of concept has been successful on Silicon-On-Insulator (SOI) featuring a nano-film device layer, physical devices are generally considered to require materials with thicknesses beyond the nanoscale. Significant growth is expected in the area of microharvesting - supporting the development of thin-film based thermoelectric devices - however nano-film materials offer little utility for even these smallest of thermoelectric applications. The successful demonstration of comparably reduced thermal conductivity in upscaled materials more than an order of magnitude thicker offers significant benefits for the translation of fundamental research into emerging applications.

2. ***Development of an approach allowing free standing defect engineered silicon to be produced without a requirement for an isolating layer of buried oxide.*** The defect engineering approach applied by Bennett et al created vacancy rich device layers with significantly reduced thermal conductivity by taking advantage of an isolating layer of buried oxide present in SOI wafers. This layer acts to prevent interregional defect migration, effectively preventing local recombination of vacancy and silicon interstitial. Such material however presents challenges for utilisation in devices. An alternative approach is required if vacancy rich material is to be produced without a requirement for this isolating layer. A new method is developed and then experimentally tested to determine whether reductions in thermal conductivity can be successfully translated to free standing material.

3. Development of a means of obtaining thermal conductivity measurements on defect engineered samples. The determination of thermal conductivity is crucial for this work as it is for many areas of fundamental research. Accurate measurement using pre-existing methods can be considered highly challenging. While micro-Raman spectroscopy has been demonstrated to enable effective non-contact, non-destructive estimation of thermal conductivity, significant limitations in accuracy were identified. Furthermore, this approach presented physical limitations for nano- and thin-film materials. Measurement on samples that did not meet thickness requirements or that were installed on substrates or supporting structures were not possible leaving alternative approaches that can compromise samples and which require relative complexity in experimental design and analysis. An analytical model was developed during this work to address these challenges. A straightforward non-contact, non-destructive approach using micro-Raman spectroscopy with significantly improved accuracy was complimented by the removal of existing limitations around sample thickness and substrate presence. Firstly, the influence of any substrate or supporting structure on obtained results could now be accurately established; an improvement over a “*rule of thumb*” approach previously applied and which was shown to be insufficient. Secondly, estimations of sample only thermal conductivity could now be calculated where an influence from substrate was determined. This new model offers significant value to experiments undertaken in this thesis and to other researchers with an interest in this material property.

1.3 Novelty of this Work

This thesis investigates the upscaling of vacancy defect engineering for the purposes of reducing thermal conductivity in c-Si for thermal energy harvesting applications. Several areas of novelty are presented. **(i)** Only a single proof of concept study has been reported in the area of vacancy defect engineering for this purpose in silicon, with successful reductions achieved in 100 nm thick SOI device layers with n-type dopant. While potential for upscaling was suggested, this thesis demonstrates the first experimental efforts to do so. Material approaching 2 μm thick is produced and effects on thermal conductivity reported. **(ii)** No direct confirmation has yet been presented of vacancy defect concentrations and reduced thermal conductivity in the one sample. It has only been theorised that they are present. This work is the first to investigate the presence of vacancy concentrations and changes to thermal conductivity together in defect engineered c-Si. **(iii)** Both n-type and p-type materials are investigated, allowing

comparative evaluation of effects and the reporting of outcomes for both doping types frequently used in thermoelectric applications. This work is the first to undertake vacancy defect engineering for the purpose of producing a low thermal conductivity thermoelectric material on p-type samples at any thickness. **(iv)** Existing methodology for the creation of vacancy rich material using ion implantation utilised the isolating effects of a layer of buried oxide for success. Thermoelectric materials with such isolating layers present challenges for straightforward application to thermoelectric devices. A method to produce vacancy rich material without any requirement for this isolating layer was developed and tested in this work for the first time. Free-standing c-Si thin-film samples with a thickness of $2\ \mu\text{m}$ and containing large concentrations of vacancy defects were produced and effects on thermal conductivity versus the approach using an isolating oxide layer investigated. **(v)** A new model allowing non-contact, non-destructive measurement of thermal conductivity using micro-Raman spectroscopy was reported during this work. Accuracy was improved by a factor of 2 over a previous approach and an extension allowing estimates of sample only thermal conductivity to be obtained for samples on substrates or installed *in-situ* was developed. No straightforward method to accurately determine substrate influence on measurement results nor to determine sample only thermal conductivity where influence was present had previously been possible. Such an approach offers significant utility not only in this work but to the broader research community.

Chapter 2: Literature Survey

2.1 Introduction

The work contained in this thesis is focused on the engineering of vacancy defects within silicon, manipulating its intrinsic properties of thermal conductivity so that it may be used effectively for thermoelectric energy harvesting applications. The following chapter presents a literature survey of relevant research in the field of thermoelectrics, providing an introduction to thermoelectric power generation and detailing the complex nature of thermoelectric materials. The survey then focuses on the application of silicon within this field, presenting the key research reported in this area and highlighting opportunities. It is in pursuit of such opportunities that the work presented in the remainder of this thesis is dedicated.

2.2 An Overview of Thermoelectric Devices

Thermoelectric devices have seen reliable use for over 4 decades. Benefiting from solid state construction, and with an ability to produce electricity directly from heat or to pump heat under reversed conditions, such devices have been utilised where packaging, access or operational conditions demand reliable, small scale, maintenance free generation or cooling.

While thermoelectric devices offer low levels of efficiency compared to more conventional heat engines - leaving them unsuitable for large scale generation - their scalable nature makes them highly suitable in energy harvesting roles. The opportunity for compact device sizing combined with a lack of moving parts has seen thermoelectric devices traditionally feature in both military and aerospace applications. Current commercial devices typically offer efficiency levels $< 7\%$ [16, 17] leaving scope for even moderate improvements in material performance to deliver a sizeable impact.

Radioisotope power systems - harvesting energy from a high particle source via a thermoelectric generator - remain at the forefront of NASA's space power solutions. Multi-mission radioisotope thermoelectric generators (MMRTG) suitable for deployment in both Space and Mars environments are currently active while research is underway to develop a next-generation enhanced multi-mission package. Curiosity Rover is equipped with an MMRTG producing an electrical power output of 110W from a thermal power output of 2000W [18, 19]. High Temperature Solar

Thermoelectric Generators targeting future operation in deep space exploration are expected to exceed 15% efficiency for temperatures in the range of 1000°C [20, 21].

A move towards wearable technology, remote sensors and the need to provide battery trickle charging in a range of modern devices is expected to enable thermoelectric devices to play an increasing role in tomorrow's wireless connected products and consumer electronics. By 2024, growth in these sectors was expected to surpass the current demand for thermoelectric generators provided by the military and aerospace sectors by several orders of magnitude [22]. Such progress has yet to be realised, at least in part through a disconnect between application needs and material design.

Commercial devices targeting terrestrial sources of waste heat remain dominated by materials such as Bismuth Telluride (Bi_2Te_3) and Lead Telluride (PbTe) despite an abundance of new materials under research. Although reporting a potential for higher levels of performance and availability, these new materials have yet to prove suitable for manufacture or processing on a scale required for commercial uptake. The breakthrough to the next generation of high efficiency, commercially suitable materials remains to be found.

2.3 Thermoelectric Effect

Fundamental to all thermoelectric materials is the generation of an electromotive force in response to a temperature gradient.

Charge carriers present within the thermoelectric material can be described as diffusing in response to heat. When provided with a temperature gradient across the material, the diffusion and subsequent build-up of these charge carriers towards the colder side is found to generate an electromotive force in proportion to the temperature difference present.

This effect is known as the Seebeck effect; with the proportional change in voltage, U produced in response to this temperature difference known as the Seebeck coefficient.

Discovered in 1821-3 by Thomas Johann Seebeck, this effect can be expressed by:

$$U = S \Delta T \tag{2.1}$$

where S is the Seebeck coefficient and ΔT is the temperature difference present across the material.

2.4 Thermoelectric Power Generation

The Seebeck effect can be utilised to design thermoelectric devices capable of power generation. Conventional device architectures currently in use by commercial applications seek to take advantage of the difference in the voltage polarity produced by n- and p-type materials. These n-type materials possess an abundance of negative charge carriers (electrons) while p-type materials are those with an abundance of positive charge carriers (holes). By electrically connecting the hot ends of a pairing of n- and p-type materials and placing a load across the cold end of the same pairing, the provision of a temperature gradient and heat flow through the pairing can be used to effectively generate power. This configuration of n- and p-type materials assembled in combination can be seen in Figure 2.1.

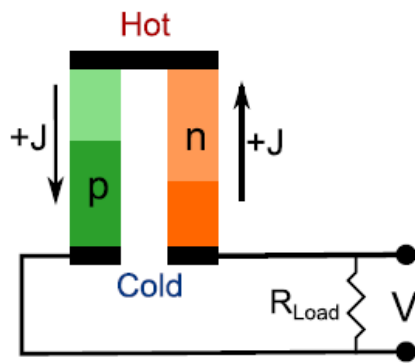


Figure 2.1 Thermoelectric power generation using a pairing of n- and p-type materials. These n- and p- type materials are connected electrically at the hot side, with the load placed across the ends at the cold side. The cold side ends are connected electrically only via the load. +J shows the positive charge direction.[23]

By comparing such a pairing to an ideal voltage source, it can be seen that multiple pairings may be combined to allow increased power to be produced via increased voltage and/or current. Devices can therefore be designed to meet a range of user requirements and specific applications.

By reversal of the operational conditions utilised for the production of power, thermoelectric devices may also operate as a cooler – or heat pump – rather than a generator. The application of a power source to the legs of the device in place of a load produces an effect whereby heat is either absorbed or rejected at the electrical junction of the leg pairing. This effect, known as the Peltier effect, provides for a Peltier coefficient representing the relationship between the amount of heat carried across the device and the current passed through it.

Away from device architectures currently deployed commercially, breakthrough research has reported success with thermoelectric devices using only a single charge type material [24]. These unipolar devices offer distinct advantages over conventional

architectures, negating a need to manufacture two distinct materials and providing a simple solution to the challenge of matching properties of n- and p-type elements faced in device design.

Total power, P , produced by a given thermoelectric device can be expressed in the form of $P = \frac{U^2}{R}$ by substituting the Seebeck coefficient and temperature terms from equation (2.1) to give:

$$P = \frac{S^2 \Delta T^2}{R} \quad (2.2)$$

Expressing R , resistance in terms of electrical resistivity, ρ , where:

$$R = \rho \frac{l}{A} \quad (2.3)$$

with A representing cross sectional area of the thermoelectric element(s) and l their length, allows equation 2.2 to be given as:

$$P = \frac{S^2 \Delta T^2 A}{\rho l} \quad (2.4)$$

Equation (2.4) allows the relationship between power generation and fundamental thermoelectric properties to be readily evaluated.

To maximise power output a thermoelectric material is seen to require a high Seebeck coefficient and a low electrical resistivity. A sensitivity to temperature difference and to dimensional factors via the ratio of cross sectional area and length are also observed. This power output dependence on material properties of Seebeck coefficient and electrical resistivity can be seen in the use of the term thermoelectric power factor, represented by $PF = S^2/\rho$ for the categorisation of thermoelectric materials [25]. For both equation (2.4) and that for PF , it should be noted that properties of Seebeck coefficient and electrical resistivity are strongly temperature dependent, introducing a further overall sensitivity to physical temperature itself.

2.5 Thermoelectric Efficiency and Performance

As with all heat engines, thermoelectric devices are bound by the efficiency limits of the Carnot cycle [26]. At the device level, maximum efficiency is therefore limited by:

$$\eta = 1 - \frac{T_c}{T_h} \quad (2.5)$$

where T_c = cold side temperature and T_h = hot side temperature.

The efficiency of a thermoelectric material itself can be expressed as:

$$\eta = \frac{P}{q} \quad (2.6)$$

where q represents heat flow through the material and P represents power output resulting from heat flow, q .

With l , length considered thickness, q can be given as a function of thermal conductivity, k :

$$q = \frac{k}{l} A \Delta T \quad (2.7)$$

Combining equations (2.4), (2.6) and (2.7), a simple statement for efficiency of a given thermoelectric material can thus be written as:

$$\frac{P}{q} = \frac{\left[\frac{S^2 \Delta T^2}{\rho} \frac{A}{l} \right]}{\left[\frac{k}{l} A \Delta T \right]} = \frac{S^2 \Delta T}{\rho k} \quad (2.8)$$

Where an evaluation of equation (2.4) allowed insight into maximisation of thermoelectric power to be obtained, an evaluation of equation (2.8) allows a fuller insight into the requirements of an efficient thermoelectric material. For maximum efficiency a thermoelectric material must combine the large Seebeck coefficient and low electrical resistivity identified for maximised power generation identified in equation (2.4) with a low level of thermal conductivity. As was the case when evaluating power, caution is also required when seeking to understand thermoelectric material efficiency. All three material properties contained in equation (2.8) display strong temperature dependences. As with Carnot cycle limits shown in equation (2.5), results obtained using equation (2.8) are shown to be further influenced by the magnitude of the temperature difference applied during any measurement process. This combination of influences from i) temperature gradient and ii) the temperature dependence of material properties can present challenges when evaluating the thermoelectric potential of a given material.

2.6 Evaluating Thermoelectric Performance

The use of alternative approaches as a means to mitigate these challenges - particularly sensitivity of results to magnitude of temperature gradient - appears in literature but each reveals shortcomings. Categorising material performance remains problematic as a consequence. Two key methods however are most frequently applied.

2.6.1 *Figure of merit, zT*

The factor zT commonly referred to as the “figure-of-merit” features ubiquitously in the evaluation of thermoelectrics [27]. By replacing the temperature difference ΔT given in equation (2.8) with a mean temperature \bar{T} , obtained via $[(T_h + T_c)/2]$ the figure-of-merit can be given as:

$$zT = \frac{S^2 \bar{T}}{\rho k} \quad (2.9)$$

While this approach successfully removes any sensitivity to the magnitude of temperature gradient available during measurement, a fundamental sensitivity to temperature nonetheless remains. Firstly through the strong temperature dependence of material properties relating to Seebeck coefficient, electrical resistivity and thermal conductivity and secondly as a consequence of values obtained for zT now being the product of mean temperature itself. Such an approach presents significant limitations when undertaking performance evaluation. Values obtained for zT can potentially be increased by simply increasing measurement temperature. Indeed it is no surprise that high zT materials tend to be represented by those with high operating temperatures. In addition, any loss in basic performance at this increased temperature - readily discoverable during application - has the potential to be obscured providing it remains smaller than the magnitude of the gain in mean temperature introduced.

2.6.2 *Evaluation using z*

An alternative solution is offered by evaluation of performance using the term z , where $z = S^2/\rho k$. Such an approach is arguably an improvement over the approaches offered by equations (2.8) and (2.9). The value returned is no longer the product of either temperature gradient or mean temperatures present during measurement offering a clearer insight into the relationship of fundamental material properties themselves.

Nonetheless, the inherent sensitivity to measurement temperature of these fundamental material properties remains.

2.6.3 Practical implications

While discussion is given in literature to challenges around evaluation [27, 28], and the usefulness of zT when power generation is a dominant objective [29], a solution at present remains unrealised. The wide range of operating temperatures offered by an increasingly diverse range of reported thermoelectric materials impedes approaches such as standardised measurement conditions from being applied in a practical manner.

Despite these drawbacks, expressing material characteristics in relation to performance efficiency remains in common use. Reported results continue to attempt to provide some means by which thermoelectric performance may be readily quantified and directly compared. The use of such metrics should however be approached with caution, especially where attempts to compare performance at significantly different operating temperatures are undertaken.

Figure 2.2 shows various values of reported zT for a variety of thermoelectric materials as a function of their operational temperature range. As mentioned previously, that high values of zT are to be found accompanying high operating temperatures is not unexpected.

From Figure 2.2 it can be seen that the 3 materials with a history of commercial application, namely Bi_2Te_3 , PbTe and SiGe offer similar zT values, ~ 1 , but for quite different temperature ranges. SiGe achieves its peak zT at $\sim 1200\text{K}$, a temperature considerably higher than the $\sim 350\text{K}$ of Bi_2Te_3 or the $\sim 600\text{K}$ of PbTe . It can be further noted that while SiGe reveals a broadly linear increase in zT with temperature, both Bi_2Te_3 and PbTe display significant reductions in values of zT as temperature is increased beyond optimal. Such a reduction indicates a significant drop off in performance parameters for temperatures greater than maximum zT given the role of the temperature term in the figure-of-merit equation. This disparity in behaviour readily highlights the additional challenge of attempting to undertake comparative evaluation of thermoelectric materials through a universal term. Information crucial to application is lost, while materials may risk comparison against others with which they share no practical commonality.

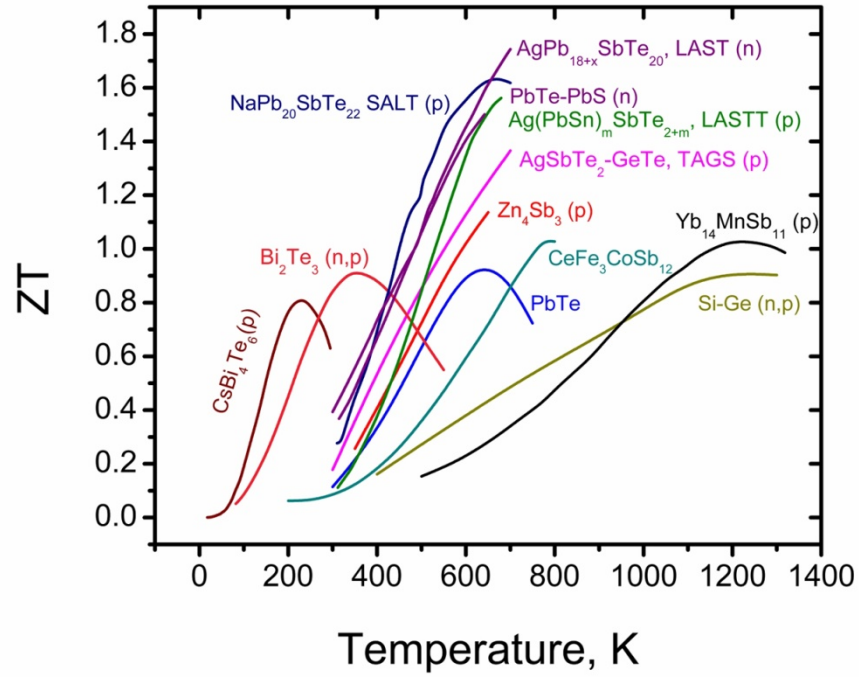


Figure 2.2 Figure of merit, zT , for various reported thermoelectric materials as a function of temperature. [30]

2.7 Conventional Design of Thermoelectric Materials

The fundamental challenge of thermoelectric materials has historically been considered one of finding balance between interdependent and often conflicting properties. Equation (2.9) for the figure-of-merit reveals the significant challenges that exist for material design. For efficient performance, a good thermoelectric material must combine a large value of Seebeck coefficient with low values for electrical resistivity and thermal conductivity.

2.7.1 Electrical properties

The presence of a single, dominant type of charge carrier - important if a large Seebeck coefficient is to be obtained - must be considered in conjunction with the number (or concentration) of charge carriers themselves. While a large charge carrier concentration can be considered good for electrical conductivity, Seebeck coefficient typically shows a reduction as carrier concentrations increase. Balancing this relationship is further complicated by the squaring of the term for Seebeck coefficient in the calculation of power.

An understanding of this interdependent relationship between Seebeck coefficient and electrical conductivity can be had by evaluating relevant equations [31-33]. Expressing both properties in terms of carrier concentration, n , a simplified transport equation for Seebeck coefficient can be shown as:

$$S = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{2/3} \quad (2.10)$$

where k_B is the Boltzmann constant, e is the carrier charge, h is Planck's constant and m^* is the effective mass of the charge carrier.

While electrical conductivity, σ , can be given as [31, 33] :

$$\sigma = ne\mu \quad (2.11)$$

where μ is the carrier mobility and e is the carrier charge.

Any increase in carrier concentration can thus be expected to produce an increase in electrical conductivity while simultaneously acting to reduce Seebeck coefficient. For reductions in carrier concentration, the inverse holds.

The effects of this relationship can be clearly seen in Figures 2.3 and 2.4. These figures present electrical resistivity and Seebeck coefficient for a variety of n- and p-type doped silicon and SiGe materials as a function of carrier concentration.

In Figure 2.3 resistivity is shown to reduce as carrier concentration is increased for each material considered. With electrical resistivity the reciprocal of electrical conductivity, electrical conductivity can be understood to be increasing if resistivity is decreasing. Such findings are in line with expectations as per equation (2.11).

Figure 2.4 reveals that corresponding increases in carrier concentration are shown to result in decreases in values of Seebeck coefficient in line with equation (2.10). Such behaviour is found for all materials presented within the figures, irrespective of dopant and dominance of either n- or p-type charge carrier types.

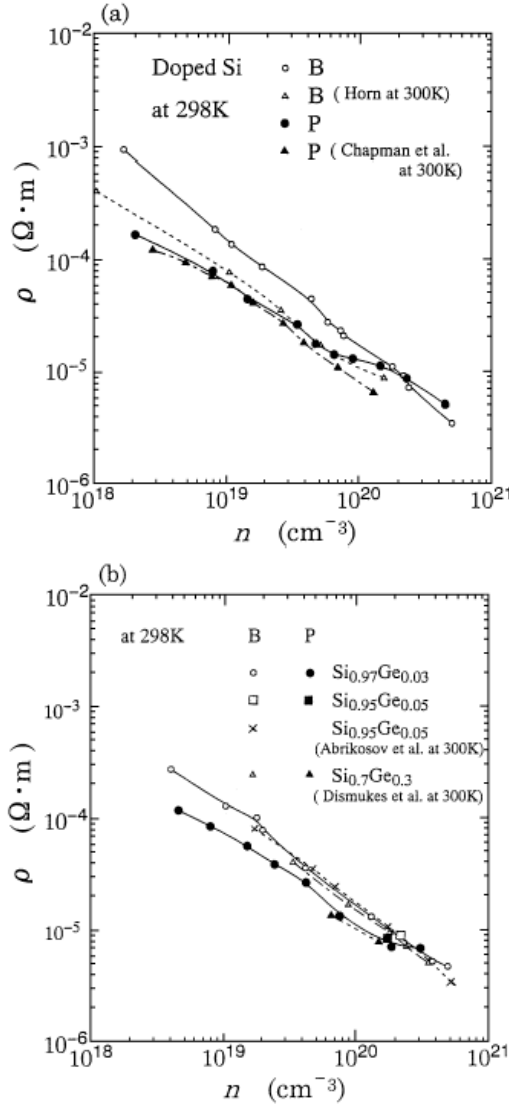


Figure 2.3 Electrical resistivity in response to increasing carrier concentration for doped Si (a) and SiGe (b) material of both N and P type.[34]

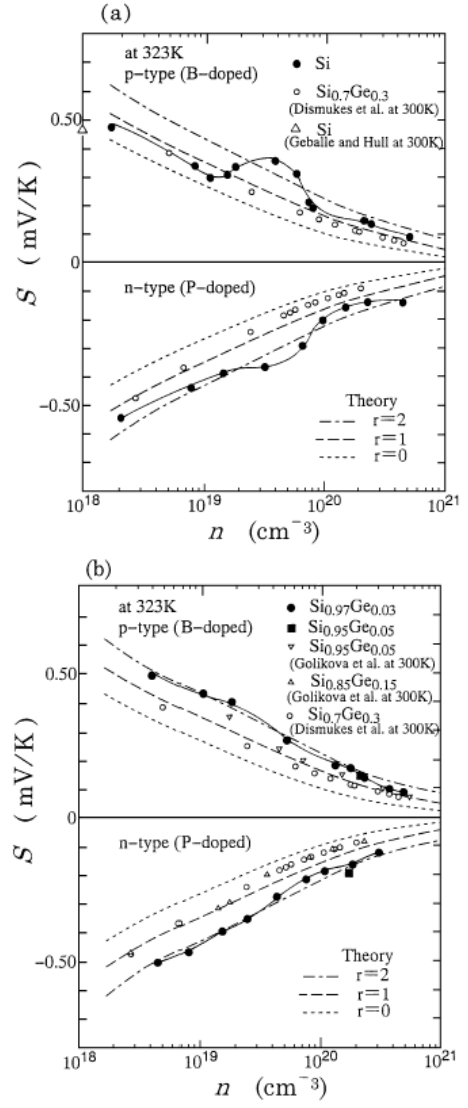


Figure 2.4 Seebeck coefficient in response to increasing carrier concentration for doped Si (a) and SiGe (b) material of both N and P type.[34]

2.7.2 Thermal conductivity

Equation (2.8) establishes a clear relationship between high thermal conductivity and reduced levels of thermoelectric efficiency. The contribution of thermal conductivity should ideally be minimised if high thermoelectric efficiency is sought.

In semiconductors, thermal transport consists of two mechanisms; heat transferred by charge carriers themselves as they diffuse from the hot side to the cold side, k_e and that transferred via a materials lattice structure, k_l [35]

The relationship of this electronic transport and lattice structure contributions to overall thermal conductivity can be shown thus:

$$k = k_e + k_l \quad (2.12)$$

For thermoelectric applications, this dual component nature of k is highly significant. Firstly, it presents a practical lower limit for reduction of k since carrier diffusion is fundamental to the production of a Seebeck voltage. Thermal conductivity can be reduced only so far as $k \approx k_e$ if the Seebeck effect is to be preserved. Secondly, a degree of freedom is introduced allowing reductions in k to be targeted without impact on electrical performance through reductions in the term k_l .

In solids, the concept of temperature requires the idea that atoms have motion. Atoms within a solid are found to oscillate about their equilibrium positions with an energy governed by this temperature. This oscillation acts locally upon adjacent atoms causing a corresponding vibration and vice-versa. This vibrational motion produces travelling waves capable of travel through the lattice (and thus the solid) itself. Responsible for material characteristics such as heat capacity and thermal conductivity, these travelling waves can be quantized and termed phonons. Were phonons perfectly transmitted, thermal conductivity would be infinite. That this is not the case for practical materials suggests that instead of perfect transmission, phonons experience some level of interference during travel. Typically this interference occurs through interactions with the physical boundaries of the solid, defects within the solid or by phonon-phonon interactions termed Umklapp processes.

This scattering of phonons within solids introduces a concept of phonon mean free path. Phonon mean free path can be defined as the mean distance a phonon can travel before experiencing such interference. It can be seen that reducing the length of this mean free path can be expected to increase the amount of scattering and thus reduce thermal conductivity. It should come as no surprise therefore that reducing mean free path length is of significant focus for thermoelectric research. While Umklapp processes are temperature dependent anharmonicities, acting to reduce length as temperature is increased, control over boundaries and both the number and type of defects offer a practical opportunity for material tuning.

2.8 Thermoelectric Materials

Bulk materials have traditionally formed the core of thermoelectric research, with current commercially available devices dominated by materials such as Bi_2Te_3 and PbTe . While these materials have shown acceptable levels of performance to date, they

offer little opportunity for further performance gains in this form. The alloying of these materials with further elements however provides opportunity for reduced thermal conductivity and improved thermoelectric potential. The introduction of new elements to the lattice structure of the alloy acts to create increased phonon scattering and reduced lattice thermal conductivity [36]. Improvements achieved by alloying PbTe in this way are readily identifiable in Figure 2.2. Silver and antimony based alloys of PbTe (shown as SALT, LAST and LASTT) offer zT increases of over 60% when compared to traditional PbTe free of alloying induced reductions in mean free path length.

In addition to alloying, the application of defect engineering is identified as a strategy for further thermoelectric optimization in PbTe materials [37]. Point defect scattering is shown to effectively reduce phonon mean free path length in PbTe, acting to significantly restrict phonon thermal transport. This atomic scale phonon scattering introduced via point defects is not only restricted to PbTe. Effects can be achieved almost universally in thermoelectric materials. For example significant scattering of short wavelength phonons by point defects is reported by Zhu et al using SiGe material [38]. As a result of this ubiquity, He & Tritt identify multiscale defect engineering as being one of three emerging areas key to the development of next generation materials during their review of advances in thermoelectric materials [11].

Away from commercial materials, thermoelectric research can be summarised as fragmented. A lack of cohesive leadership or unifying vision leading to a research landscape with a large variety of materials. Numerous review papers exist offering insight into advancements in materials such as clathrates [39], skutterudites [40], heusler and half-heusler [41], oxides [42], electrically conducting organic materials [43] and graphene [44]; with research objectives frequently focused solely on increasing zT . While such materials are not reviewed in this overview, these many review papers offer an interested reader an excellent starting point for further investigation.

2.8.1 High zT performance

A high zT of 1.7-1.8 was reported using Cu_{2-x}Se bulks at a temperature of $\sim 973\text{K}$ [45], while an unprecedented zT of 2.6 ± 0.3 was achieved using SnSe crystals at a temperature of 923K [46]. As previously discussed, the inherent sensitivity of zT to high measurement temperatures suggest that caution should be taken when viewing

such results in a broader context. A calculated best value of z for these high zT reported SnSe crystals can, for example, be approximated to $2.8 \times 10^{-3} \text{ K}^{-1}$. This value is in line with that of Bi_2Te_3 , a current commercial material with a much lower value of $zT = 1$ and a peak performance temperature of $\sim 350\text{K}$. Potential avenues for ultra-high performance thermoelectric devices exploiting materials where a high zT is achieved via high operating temperature should therefore be viewed cautiously.

Theoretically, significant increases in zT can also be achieved through combined effects of quantum confinement and reduced thermal conductivity. Using values for PF in Bi nanowires[47], and applying theoretical values for thermal conductivity, theoretical limits of $zT > 6$ are considered possible.[48] The practical realisation of such materials is however challenging.

2.8.2 Silicon compound thermoelectric materials

Classically, the use of silicon as a potential thermoelectric material has been restricted to silicides and silicon-germanium.

Silicon Germanium has seen use as a thermoelectric material in space missions and exploration as a component of radioisotope power systems. In these systems the heat source is provided by decay of radioactive isotopes offering long term continuous operation. SiGe based thermoelectric generators can operate at high temperatures. Joshi et al reported a figure of merit, $zT = 0.95$ for p-type nanostructured SiGe at 800°C [49]. Such results represent a performance increase by a factor of 2 over bulk SiGe alloys in use at the time. In this material, nanostructuring was responsible for an almost 50% reduction in thermal conductivity while a modest increase in power factor was also noted.

Silicides and their thermoelectric potential have been studied since 1958 with devices successfully produced in both modern and historical periods of thermoelectric interest.[50] Formed by combining silicon with a variety of metals, silicides provide stability and potential for both n- and p-type material with reasonable levels of zT .

Review papers by Nozariasbmarz et al [51] and Fedorov & Isachenko [52] offer insight into progress in thermoelectric silicides. While a broad range of silicides are shown to be of research interest for thermal energy conversion, most offer optimal performance at temperatures $> 500\text{K}$. Manufacture of devices for such operating temperatures requires high temperature solutions, while opportunities for sources of waste heat at such

temperatures in identified growth areas of consumer electronics and wearables can be considered minimal.

Nonetheless, some silicides do offer promise for application in the <500K range. Magnesium silicide alloys doped with tin offers a zT of almost 0.5 at 300K [53].

A current range of thermoelectric suitable silicides is shown in Table 2.1 where composition, melting point and maximum measured zT are detailed. Despite advances, present performance of these silicides remains below that typically provided by competing materials in current commercial use. While suitability for operation at temperatures greater than 500K offers potential utility, recent developments in high temperature thermoelectric generators have instead utilised skutterudite materials[54, 55] leaving the future for silicides unclear.

Table 2.1 List of metal silicides offering potential use in thermoelectric applications and their parameters

Material	Melting Point (K)	Type	Maximum zT
CrSi ₂	1763	p	0.25
MnSi _{1.7}	1430	p	0.7
FeSi ₂	1490	n	0.2
FeSi ₂	1490	p	0.2
Ru ₂ Si ₃	1970	n	0.4
Ru ₂ Si ₃	1970	p	0.27
CoSi	1700	n	0.2

Source : [50]and individual references therein.

2.8.3 Nanoscale approaches

A key approach in modern thermoelectric material design, the application of nanoscale effects to thermoelectric materials offers strong opportunities for enhanced performance. Classically, nanoscale approaches involved the use of low-dimensional materials featuring scale lengths in the order of 10^{-9} m. Hicks and Dresselhaus predicted in 1993 that design of low dimensional materials for thermoelectric purposes could enhance performance [6, 7] and this prediction has been proven by real world results in the years since [56]. More recently however, the development of dimensionally bulk materials containing nanoscale effects has resulted in an expansion in usage of this term.

Nanocrystalline materials, with a material morphology a mixture of nanometre grains and associated interfaces offer potential for significant performance over similar

materials without nanostructuring [49]. Such materials possess low thermal conductivity as a result of significant phonon scattering sites and an inherently low phonon mean free path. Of significant interest in such materials is the potential energy dependence of the interaction between charge carrier and grain interfaces [57]. Simultaneous increases in values of both Seebeck coefficient and electrical conductivity in contravention of behaviour in conventional materials have been reported [58, 59].

Similar effects on reduced phonon mean free path are reported in bulk nanostructured materials. Semiconductor materials such as skutterudites, clathrates, heusler and half-heusler alloys incorporate various nanoscale defects such as voids, rattlers, intergranular phases and grain boundaries to enable a reduction in the mean free path length of phonons. These nanostructures act to introduce selective scattering and reduce thermal conductivity [60]. Opportunities for metamaterials further add to the expanding use of this term, allowing material with dimensions approaching thin-film or bulk scale to be created from repeating structures of distinctly identifiable nanometre scale units. These structures, such as nanowire arrays and superlattices enable classical low-dimensional strategies targeting phonon scattering and power factor enhancements to be exploited in materials with overall dimensions more suitable for device application [12]. Wan et al reported thermoelectric power factors in a flexible superlattice constructed of hybrid inorganic-organic materials. Such material allowed electron density to be reduced for one component through heating, while structural integrity was maintained by a second material with a higher boiling point [61].

2.9 Silicon as a Thermoelectric Material

Silicon features as an important material in thermoelectric research. Thin-film thermoelectric generators with active device thicknesses of 1-20 μm are predicted to find a growing number of applications through the powering of one-way communication devices and wearable electronics. For such applications, power requirements are expected to be low – in the order of 1 mW – allowing practical utilisation of energy harvesting as an energy source. Highly doped silicon possesses a PF favourable for such applications. As an abundant, non-toxic material with significant manufacturing know-how, this unique combination of properties offer significant benefits - particularly where volume based products are required. Such strengths are further enhanced by a low material cost. Silicon is approximately 36 times cheaper per kg than current commercial alternatives such as Bi_2Te_3 [62].

Despite these strengths, utilisation of silicon as a thermoelectric material is negatively impacted by its relatively high level of thermal conductivity. With a room temperature value of $\sim 140 \text{ W/mK}$, zT for bulk Si is in the order of ~ 0.01 [63]. Such a value is 100 times lower than current benchmark materials with a $zT=1$. For c-Si, phonon mean path can be measured in scale lengths as large as 10^{-6} m [64]. While 80% of phonons are calculated to possess a mean free path $\geq 10 \text{ nm}$ [65], both calculation and experiment suggest that significant thermal transport is undertaken by phonons with mean free path lengths $> 100 \text{ nm}$ [66]. At room temperature, $\sim 40\%$ of c-Si thermal conductivity was determined to be resultant from phonons with a mean free path length $\geq 1 \mu\text{m}$ [67].

Perhaps unsurprisingly, nanoscale approaches targeting effective reductions in phonon mean free path length and/or increased scattering have significant potential in the development of silicon thermoelectric materials. Haras et al [68] offers clear insight into this potential, reporting the effect of changes to material thickness on measured thermal conductivity. This relationship can be seen in Figure 2.5, where k is presented as a function of silicon film thickness. Silicon with a film thickness of $\sim 10 \mu\text{m}$ is shown to possess a value of k typical of bulk material. By comparison, silicon films with a thickness $\leq 1 \mu\text{m}$ are clearly seen to demonstrate comparatively reduced properties, with reductions increasing as thickness diminishes. Here the reducing thickness of the film acts to reduce phonon mean free path by introducing a greater number of phonon-boundary interactions.

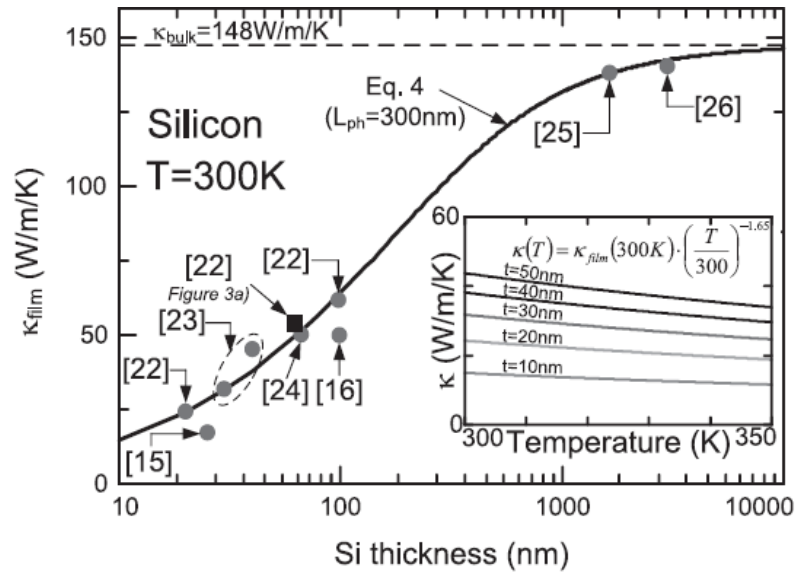


Figure 2.5 Room temperature thermal conductivity as a function of material thickness for Silicon (Source: [68] and additional references within)

Just as for non-silicon thermoelectric materials, strategies for nanostructuring of silicon thermoelectric materials can take several forms. However all predominantly seek to leverage reductions in thermal conductivity over levels typical of bulk silicon. Development of silicon nanowires [8, 9], porous meshes [69], and nanocrystalline bulk films [70] all with low levels of thermal conductivity offer significant potential as thermoelectric materials.

2.9.1 Silicon nanowires

The development of silicon nanowires, where dimensional confinement in the cross sectional plane can be achieved using widths in the order of 10^{-9} m, enables extreme exploitation of the thermal conductivity – material thickness relationship presented in Figure 2.5. Boukai et al [9] and Hochbaum et al [8] experimentally determined significant improvements in zT possible using nanowires by evaluating single nanowires from a thermoelectric perspective. A value of $k \cong 1.6$ W/mK at room temperature was reported for 52 nm nanowires manufactured using electroless etching [8]. Such a value approaches that of amorphous bulk SiO_2 [71] and the lower limit of 1 W/mK predicted by [72] for silicon thermal conductivity. This work, which reported a best $zT = 0.6$ at room temperature, contained several important findings for the future direction of silicon nanowires. While reductions in k were shown to be sensitive to nanowire thickness, confirming expectations about phonon-boundary scattering and a reduced phonon mean free path length; results were also found to be sensitive to manufacturing technique. Nanowires manufactured using an electroless etching method displayed greater reductions in k than those grown using a vapour-liquid-solid approach. For example room temperature thermal conductivity of a 115 nm nanowire manufactured using an electroless etching approach was found to be ~ 8 W/mK, compared to ~ 42 W/mK for a comparable 115 nm nanowire grown using a vapour-liquid-solid method. Such comparative differences, although unexpected, were repeated for all nanowire sizes investigated. A significant disparity in surface roughness between the two types of wires was noted, and a hypothesis presented suggesting that effects of surface roughness on phonon transmission were a likely cause of these unexpectedly low values.

These findings are in line with results presented elsewhere. Li et al reported a comparable thickness dependence to thermal conductivity in smooth nanowires, with $k \cong 6$ W/mK for a 22 nm nanowire, and $k \cong 42$ W/mK for a 115 nm wire; both at room

temperature [73]. Zhang et al reported values of thermal conductivity on silicon nanowires combining smooth and rough surfaces with and without porosity [74]. Smooth, non-porous nanowires returned a room temperature $k = 19.74$ W/mK, while rough, porous nanowires were found to yield a value for $k = 1.68$ W/mK. The effects of porosity on thermal conductivity can be readily understood by considering the presence of pores as analogous to defects from a phonon transport perspective. A direct connection can then be seen between an increase in the number of sites capable of producing phonon scattering and a reduction in thermal conductivity itself. The influence of surface roughness on thermal conductivity is however less obvious. An explanation is offered by Heron et al [75]. The measurement of thermal conductivity on nanowires was undertaken at low temperature in order to determine the effects of size on phonon transport. Results demonstrated that surface roughness played an important role at the nanoscale. Smooth surfaces were determined to be reflective to phonons, allowing their continued transport and effectively increasing mean free path length. Rough surfaces meanwhile were found to prevent this reflectance providing average roughness was greater than the dominant phonon wavelength. While low temperatures were used for experimentation, this behaviour can be generally considered present also at higher temperatures. This interaction of phonons with surface roughness, acting to disrupt phonon reflectance and reduce phonon mean free path length provides explanation for the enhancement reported by Hochbaum et al and others.

Review papers such as [76] and [28] offer further insight into the broad range of research undertaken on silicon nanowires for thermoelectrics. Pennelli in particular provides important insight into the balancing of electrical properties alongside the potential for reduced thermal conductivity in such material [28]. For highly doped silicon, electrical conductivity is shown to be insensitive to changes in nanowire width above 20 nm. With electrical conductivity minimally sensitive to surface roughness, discussion suggests that nanowire sizes > 20 nm are well suited to targeting with surface roughness in order to maximise thermoelectric potential.

Beyond nanowire thickness and surface roughness, research by Bennett et al [13] found that dislocation loops introduced to the nanowires could be used to increase thermoelectric power factor. These dislocation loops were hypothesised to introduce a filtering of low energy carriers, resulting in an increased Seebeck coefficient. With dislocations showing no effect on thermal conductivity, these findings offer an

interesting opportunity for additive combination with control of nanowire thickness and surface roughness for thermoelectric application.

2.9.2 Porous silicon

The study of material featuring internal nanopores offers a further avenue for the development of silicon thermoelectrics. Early experiments determined a significantly low thermal conductivity for porous silicon structures [77]. 31 μm thick layers featuring high levels of porosity - between 64% and 89% - were found to return values of thermal conductivity at room temperature of $< 0.2 \text{ W/mK}$. These values are in good agreement with theoretical models suggesting significant restrictions to phonon mean free path are introduced by large numbers of nanometre size pores. Theoretical work undertaken by Yang et al suggested that thermal conductivity in two-dimensional nanocomposites was influenced by both the volume fraction of cylindrical pores and their radius[78]. For any given porosity, smaller pore diameters were predicted to produce lower effective thermal conductivity than larger pore diameters as a result of additional surface scattering. Computation of performance on nanoporous silicon reported by Lee et al expanded this work to a fuller evaluation for thermoelectricity[79]. Size and shape were investigated and found to be determinants in phonon scattering. Smaller pores were again found to outperform larger ones; and circular pores were found to produce lower values of k than square pores. This influence of shape on scattering is somewhat at odds with conclusions presented by Liu and Huang. An array of shapes were tested for effective reductions in thermal conductivity in silicon at micro- and nanoporous scales with circular pores were reported as the worst performing of shapes tested. Triangular pores were predicted to produce greatest phonon diffusion [80].

Simulation of phonon transport in two-dimensional porous silicon undertaken by Hao et al reported that significant reductions in thermal conductivity could be achieved even with pore sizes measurable in microns[81]. The conclusion that frequency dependent phonon mean free paths are important in understanding the complex picture of thermal transport in silicon is in line with findings from Minnich et al [66] and Regner et al [67] where phonons with wavelengths spanning 100nm to $> 1 \mu\text{m}$ were found to contribute significantly to thermal conductivity at room temperature.

Reductions in electrical conductivity over bulk were noted for porous structures by Lee et al [79], with effects increasingly pronounced as levels of carrier concentrations were

increased. These reductions were noted to be a factor of 2-4 over that measured in bulk silicon with comparable carrier concentrations. A reduction significantly smaller than that presented by Yamamoto et al where electrical conductivity was reduced by several orders of magnitude as a result of porosity[82]. An understanding of these findings and the disparity in effects can be found in Aroutiounian and Ghulinyan [83]. Electrical conductivity was shown to decrease as a function of increasing porosity, transitioning from crystalline conductivity for porosity levels $< \sim 50\%$ to hopping conductivity as porosity is increased above this level. In such conditions, significant reductions in electrical conductivity are to be expected as porosity levels increase. The apparent disagreement between Lee et al and Yamamoto et al can be explainable by considering effects of differing levels of porosity, size and distribution.

Successful development of a porous film thermoelectric material has been reported by Tang et al. A “holey” silicon ribbon, 100 nm thick was manufactured to contain a honeycomb pattern of holes with uniform pitch ranging from 350 nm to 55 nm [69]. Consistent reductions in thermal conductivity were noted for all samples, however best performance was found in samples containing the smallest hole spacing. Again, large numbers of small holes proving more effective at scattering phonons than larger holes. Thermal conductivity was measured as ~ 2 W/mK, a significant reduction over the ~ 50 W/mK of non-hole samples. Such a value approaches that of amorphous material and suggests significant phonon disruption in such material. With samples found to possess good properties for electrical conductivity and Seebeck coefficient, a room temperature value of $zT = 0.4$ was returned. A notable increase over typical room temperature values for silicon of $zT = 0.01$ [63].

2.9.3 Nanocrystalline bulk silicon

Approaches for nanocrystalline bulk silicon thermoelectric materials can be considered conceptually similar to that for non-silicon materials highlighted in Section 2.8.3. The inherently low thermal conductivity of materials containing large volume fractions of nanograins can be combined with potential for counterintuitive increases in power factor resulting from energy filtering effects of the interaction between grain boundary and charge carrier.

Molecular Dynamics simulations reveal the significant potential for reductions in k using nanocrystalline silicon material. Ju and Liang suggest a room temperature thermal conductivity of $k \cong 4$ W/mK for nanocrystalline material with a grain size of 5

nm [84]. Bodapati et al meanwhile determine a strong grain size dependency to k at room temperature [85]. While a grain size of 2 nm yields an expectation of $k \cong 2.5$ W/mK, an increase in grain size to 6 nm is expected to yield $k \cong 5.5$ W/mK. In all cases, phonons are predicted to scatter at the grain boundaries while phonon mean free path length is restricted by grain size. Such values show good consistency with those experimentally reported by Bux et al [70]. A thermal conductivity of ~ 12 W/mK was achieved for doped nanostructured bulk silicon with crystallite sizes of 15.5 nm.

The potential of nanostructured bulk silicon as a practical thermoelectric material has been reported by Yusufu et al [86]. A room temperature thermal conductivity of 25 W/mK was combined with a power factor of $\sim 1.5 \times 10^{-3}$ W/mK² yielding a $zT = 0.018$ at 300K. This represents an increase in figure-of-merit over bulk silicon by a factor of 1.8. It can be noted that this power factor represents a significant increase over that reported by Bux et al for their nanostructured bulk silicon [70]. A power factor of $\sim 5.4 \times 10^{-4}$ W/mK² was reported for samples at room temperature. Power factors of 2.2×10^{-4} W/mK² [87] and $\sim 2.1 \times 10^{-4}$ W/mK² [88] have also been reported for nanocrystalline silicon films at room temperature. While seemingly in disagreement, the nanostructured bulk material manufactured by Bux et al demonstrated $k = 12$ W/mK at room temperature, resulting in a $zT \cong 0.014$. This can be compared with 3.3 W/mK for Loureiro et al and 8.5 W/mK for Acosta et al reported in [89]. Taken together, these findings demonstrate the inherent tension between the development of nanograins for effective phonon scattering and the preservation of electron transport crucial for thermoelectric application. In addition to phonon scattering, charge carriers are also found to scatter at grain boundaries reducing electron mobility [90]. For comparison, power factor in single crystal silicon was also provided by Bux et al. This was given as 2.24×10^{-3} W/mK² at room temperature. A value greater than that reported for nanostructured bulk silicon in all references above. Such comparative magnitude is in line with expectations given the lack of charge carrier scattering effects at grain boundaries within a single crystal material. These findings reveal that improvements in thermoelectric performance found in typical nanocrystalline bulk silicon materials are achieved i) via the significantly reduced thermal conductivity of the nanostructured material, and ii) at the expense of electrical properties.

The potential for nanocrystalline silicon to yield increases in power factor over that of bulk silicon however offers a possible solution. Neophytou et al reported significantly increased power factors in highly boron doped nanocrystalline silicon featuring grain

sizes of ~ 30 nm and grain boundaries of ~ 2 nm [59]. A model was presented suggesting that high electrical conductivity could be achieved simultaneously with high Seebeck coefficients through effects in the grains and grain boundaries respectively. Such behaviour is unusual, especially for bulk materials where interdependence dictates that an increase in one property produces a reduction in the other. A power factor of $15.7 \times 10^{-3} \text{ W/mK}^2$ was found in this material at room temperature. A value significantly greater than for bulk single crystal silicon or conventional nanostructured bulk materials. These findings were matched by those reported for p-type polycrystalline silicon where a power factor of $22 \times 10^{-3} \text{ W/mK}^2$ was experimentally determined [25]. Again simultaneous increases in both electrical conductivity and Seebeck coefficient were reported, and an explanation given in line with the energy filtering model presented by Neophytou [59]. With a thermal conductivity in the range of 20 W/mK [91], room temperature values of $zT = 0.33$ can be inferred. Such values are significantly lower than the above unity values hoped for in Neophytou et al [59]. Nonetheless performance values still represent significant increases over that typical for non-nanostructured materials and offer optimism for future thermoelectric applications.

2.10 Defect Engineering for Silicon Thermoelectrics

In 2011, Lee et al investigated the impact of vacancy type defects on the thermal conductivity of single crystal bulk silicon [15]. Using Non-equilibrium molecular dynamics simulations, the role of three sizes of vacancy cluster (V_4 , V_6 and V_{12}) in phonon transmission were investigated as a function of vacancy concentration. Results suggested that the introduction of these vacancy clusters could be expected to create a significant impediment to phonon transport. Thermal conductivity was predicted to reduce by $> 60\%$ following the introduction of vacancy clusters equivalent to 0.15% concentration. For greater concentrations, thermal conductivity was found to reduce further though in a non-linear manner. Maximum reductions in k were achieved for vacancy concentrations in the order of 2% . Such a reduction was shown to be a direct result of phonon-vacancy interactions. Reductions to phonon mean free path were combined with an increase in phonon scattering effects as a result of vacancy defect introduction. Values of thermal conductivity were found to be directly linked to vacancy cluster size for concentrations $< 1.5\%$. Smaller cluster size leading to increased phonon scattering rates and a greater reduction in k at such concentrations. For vacancy concentrations $\geq 1.5\%$, thermal conductivity was found to be almost

independent of cluster size; with k reduced $\sim 95\%$ over that of bulk silicon for all three sizes considered.

This predicted relationship between vacancy defect concentrations and thermal conductivity suggests significant potential for silicon thermoelectric materials. Bennett et al proposed a practical means of introducing vacancy defects at such concentrations, producing a material that was visually indistinguishable from bulk [14]. Using silicon-on-insulator with a device layer thickness of 100 nm, thermal conductivity was reduced to 6.5 W/mK without significant effect on carrier mobility or doping concentration. Electrical conductivity remained in line with that of vacancy free control samples and $zT = 0.16$ was reported at room temperature. Such a value is ~ 16 times greater than for bulk c-Si. Of importance for future research, the mechanism for this reported reduction in thermal conductivity – reduced phonon transmission via phonon-vacancy complex interaction – and the means of vacancy introduction itself are both suggested to be scalable to material thicknesses directly suitable for thermoelectric application.

2.10.1 Ion implantation induced damage

Bennett et al reported the use of high energy ion implantation as a means of vacancy defect introduction[14]. Such a process combines potential scalability with strong links to existing manufacturing capabilities. Ion implantation has seen wide use in industrial applications involving semiconductors for more than four decades, offering a controllable technique for the introduction of dopant into single crystal silicon. In such applications however its implementation is not without disadvantages. Implanted ions are typically introduced as interstitials, leaving them independent of the silicon lattice and electrically inactive. Additionally, the implantation process creates target substrate damage, negatively impacting electrical properties and substrate morphology through process induced crystalline lattice disorder and the generation of defects. At sufficient implant doses this damage can be significantly great as to cause a complete amorphisation of the target substrate itself. Caution is therefore required when designing ion implantation experiments and a post-implant rapid thermal annealing process is typically required to repair lattice disorder and allow dopant activation.

For silicon based thermoelectric applications however, this incident damage presents significant opportunities for the practical manufacture of vacancy rich material. By accelerating a silicon ion into a silicon target substrate, a cascade of associated damage can be produced within the atomic structure as the implanted ion comes to rest through

a process of nuclear and electronic stopping. Nuclear stopping involves direct collision between travelling ion and lattice site atoms. Electronic stopping involves the excitation and ionisation of lattice site atoms by the passing ion. In both cases energy is transferred from the implanted ion to the target substrate atoms. Where this energy transfer is sufficient to displace an atom from its site within the crystalline lattice a Frenkel pair is created. Each Frenkel pair consists of a silicon interstitial and a corresponding vacancy, representing respectively the displaced substrate atom itself and the now unoccupied space in the lattice structure. Displacement produced by the implanted ion is termed a primary knock-on, with each primary knock-on capable of producing further knock-on events given sufficient energy transference. A simplified image showing a single primary ion and a created Frenkel pair can be seen in Figure 2.6. With implanted ions travelling left to right, the implanted ion can be seen towards the back of the atomic lattice.

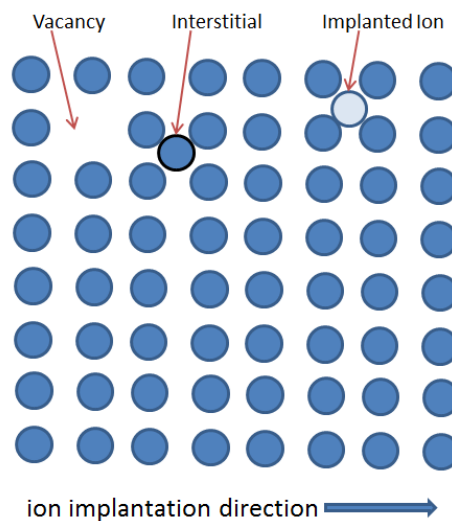


Figure 2.6 A simple lattice structure showing a single implanted ion and a corresponding Frenkel pair consisting of an interstitial atom and a corresponding vacancy site.

An average displacement energy across all lattice directions corresponding to 36 ± 2 eV is found to be required for the creation of a stable Frenkel pairing in silicon [92]. Implant energies several orders of magnitude larger than this average displacement energy are used during a typical high energy ion implantation processes. As a result, damage introduced by the highly energised ion is expected to be considerable as both primary knock-ons and subsequent knock-on events produce cascading concentrations of vacancy-interstitial pairings. Figure 2.7 offers a more representative image of the relationship between implanted ion, interstitial and vacancy. Here implantation energy for each ion is significantly greater than the average displacement energy required for

the production of a stable Frenkel pair. During such a process, large numbers of defects may be produced by a single implanted ion.

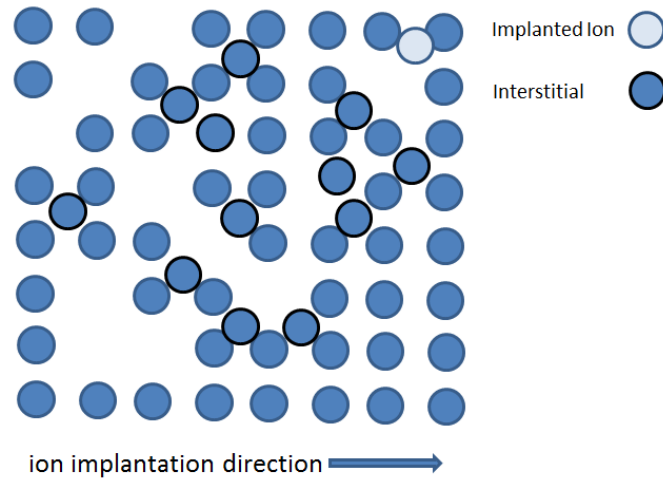


Figure 2.7 A simple lattice structure showing simplified lattice structure damage following high energy ion implantation.

2.10.2 Existing applications of vacancy defect engineering

For semiconductor processing, the presence of damage related silicon interstitials created by the implantation process can lead to detrimental performance through transient enhanced defects (TED) and dopant clustering. Where boron is used as a dopant to create p-type semiconductors, the presence of these interstitials can lead to anomalous diffusion with associated challenges in diffusion behaviour prediction and in manufacturing shallow junctions [93]. The presence of interstitials also leads to anomalous clustering as the boron forms boron-interstitial clusters – commonly referred to as BICs – rather than taking up substitutional sites in the silicon lattice [94]. These clusters reduce the concentration of electrically active boron dopant atoms. While various techniques can be employed to limit effects of TED and BIC, the use of a vacancy engineering principle has shown promise [95, 96]. By using ion implantation, a region rich in vacancy type defects can be created in the location of implanted boron dopant ions to act as an interstitial sink. Silicon interstitial saturations can be reduced and anomalous diffusion and interstitial clustering behaviours with boron dopants limited.

2.10.3 Potential scalability of the defect engineering approach

Reported findings on the depth profiling of vacancy concentrations in self-implanted silicon substrates suggest that process up-scaling of this approach for modification of

thermal conductivity has significant potential [97]. Through application of a secondary implant using gold, a depth profile was collected by taking advantage of an effect whereby gold impurities were readily trapped within regions of excess silicon vacancy defects created during self-implantation. Both distribution and concentration of the gold impurities can then be monitored in a straightforward manner using Rutherford backscattering spectroscopy. For a sample already subjected to high energy ion implantation, this approach can be used to estimate the levels of vacancy defects introduced during a high energy ion implantation process.

Figure 2.8 reveals depth profiles of gold impurity concentrations reported during demonstration of this technique. Silicon substrates are subjected to self-implantation using beam energies of 1, 2 and 8 MeV in combination with a fluence of 1×10^{16} ions/cm² before gold is added to the samples using a secondary implant. Implant energy used for the introduction of the gold impurities is 68 keV, ensuring introduction only within the surface region (~ 30 nm depth).

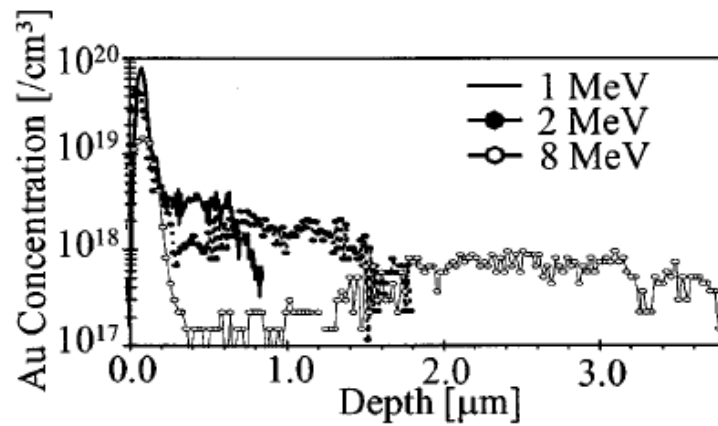


Figure 2.8 Depth profile of gold impurity concentrations reported for silicon substrates subjected to self-implantation using energies of 1, 2 and 8 MeV with a fluence of 1×10^{16} cm⁻² [97]. The gold impurities are implanted using an energy of 68 keV to ensure placement within the surface region of the silicon substrates before samples are subjected to a drive-in anneal of 1023K for 2 hours. Depth profiles are obtained using Rutherford backscattering.

Following both implantation steps, samples are subjected to a drive in anneal of 1023K for 2 hours. Significant changes in the depth distribution of the gold concentrations obtained via Rutherford backscattering spectroscopy can be seen for each of the three implant energies studied. While gold concentrations extending to a depth of ~ 0.9 μ m are found for an implant energy of 1 MeV, an implant energy of 2 MeV is shown to produce gold concentrations extending to a depth of ~ 1.75 μ m. For the maximum

implant energy used of 8 MeV, gold concentrations are shown to extend across the full 3.8 μm substrate depth presented.

While use of a low energy implant can ensure that gold impurities are located within the surface region of the target substrate - mitigating contributions of this additional implant to vacancy concentrations for the below surface regions - the use of a 1023K, 2 hour drive-in anneal used in the reported results presents significant limitations. With vacancy defects shown to be highly mobile at this temperature [98], vacancy clustering can be anticipated to occur during this drive-in annealing component. Despite this drawback, the reported results remain useful for establishing a general determination as to the potential of a high energy ion implantation based technique to be expanded to material thicknesses $\geq 1 \mu\text{m}$.

With reported findings determining 1.2 ± 0.2 vacancies per atom of gold [99] suggestive of gold impurities most likely space filling implant created vacancies, gold concentrations presented can be considered highly indicative of vacancy defect concentrations present within the target substrates following the implant and annealing process. Evaluation of Figure 2.8 letting vacancy concentration equal to 1.2 gold concentration suggests that a high energy ion implantation can be anticipated to create supersaturations of vacancy defects across materials of thicknesses significantly in excess of the 100 nm already reported by Bennett et al. With appropriate implant parameters, such a process can be expected to offer significant up-scaling potential. Material thicknesses in the range required by thin-film thermoelectric applications can be targeted.

Chapter 3: Experimental Theory and Techniques

3.1 Introduction

A variety of fabrication, processing and characterisation techniques were required in order to undertake experimental work presented in the following chapters. This chapter sets out these techniques detailing the theory behind their use and the methodologies utilised. This includes the core processes of ion implantation and rapid thermal annealing forming the defect engineering technique, alongside characterisation techniques involving morphology - positron annihilation spectroscopy and scanning electron microscopy (SEM) – and electrical characterisation. A discussion on the measurement of thermal conductivity is included within a separate chapter allowing presentation of a new approach developed during this research programme to be made.

Two differing types of silicon substrates were subjected to defect engineering and characterisation during this work. The choice of each substrate was selected to allow i) demonstration of the experimental up-scaling of this technique from a previously reported 100 nm thick silicon sample using both n- and p-type materials before ii) demonstration of application to bulk materials of thin-film thicknesses. While the specific properties of each substrate are presented in Chapter 6, a more general detail of each substrate type is given below.

3.2 Substrates

3.2.1 *Silicon-on-Insulator wafers*

Silicon-on-Insulator (SOI) wafers commonly refer to a type of silicon-insulator-silicon wafer in use by the microelectronics industry. Differing from bulk silicon wafers formed from a single, homogenous silicon crystal, SOI wafers feature a single crystal silicon device layer packaged on top of an electrically isolating layer – typically silicon dioxide – and then supported on a silicon substrate capable of manual handling.

All SOI wafers used as target substrates within this work were purchased from Ultrasil Corporation, USA and manufactured using fusion bonding. During this process, a handling substrate and surface oxide are bonded to a second substrate forming a central isolating buried layer of silicon dioxide. This second substrate is then thinned to achieve required device layer thickness.

All SOI wafers were mapped for device layer thickness by Ultrasil Corporation using a Filmetrics F50 thickness mapping system. Utilising a spectral reflectance technique, device layer thickness can be readily measured and mapped over the entire wafer surface providing a measurement of thickness and variation with an accuracy of a few angstroms. For device layer thicknesses in the order of microns, such uncertainty can be considered insignificant.

3.2.2 *Free standing silicon thin-films*

Crystalline silicon membranes featuring a free standing silicon thin-film used in this work were produced by Norcada, a company specialising in MEMS development and fabrication in Canada. Designed for use in x-ray diffraction, these membranes offer a free standing, single crystal silicon thin-film of 2 μm thickness suspended across and supported by a 300 μm thick silicon frame. These silicon membranes are manufactured using a wet etch technique comparable to [100], where anisotropic etching of the silicon material is undertaken until desired thickness is achieved.

3.3 Defect Engineering Methodology

Defect engineering represents a novel, two-step process by which supersaturations of vacancy type defects are created within target substrates using ion implantation. Significantly, materials produced are expected to be virtually indistinguishable from bulk materials. While implanted damage can be expected to significantly reduce long wavelength phonon modes contributing to thermal conductivity, high levels of implant damage are detrimental to electrical performance. By combining (i) high energy ion implantation with (ii) rapid thermal annealing, reductions in sample thermal conductivity are targeted in silicon materials without significant degradation of electrical characteristics. While the innovative process by which a sample region rich in vacancy type defects is produced is similar for both Silicon-on-Insulator (SOI) and stand-alone silicon materials, differences are sufficient to warrant separate discussion.

3.3.1 *SOI wafers*

The presence of a buried oxide layer within a SOI wafer provides a distinct advantage when seeking to produce a region rich in net vacancy defects. This layer of silicon dioxide can be penetrated by the high energy ion implantation process itself, but acts as a physical barrier to defect migration between device and handling layers during post implant annealing.

The two step process for the creation of a vacancy defect rich region within an SOI wafer can be seen in Figure 3.1. A high energy ion implant is firstly undertaken using an energy level sufficient to ensure that implanted ions - and associated damage - extend beyond the buried oxide layer separating the device and handling layers. The relative concentrations of implanted ions and associated defects following the completion of a high energy ion implantation process into an SOI wafer are detailed in Figure 3.1(a).

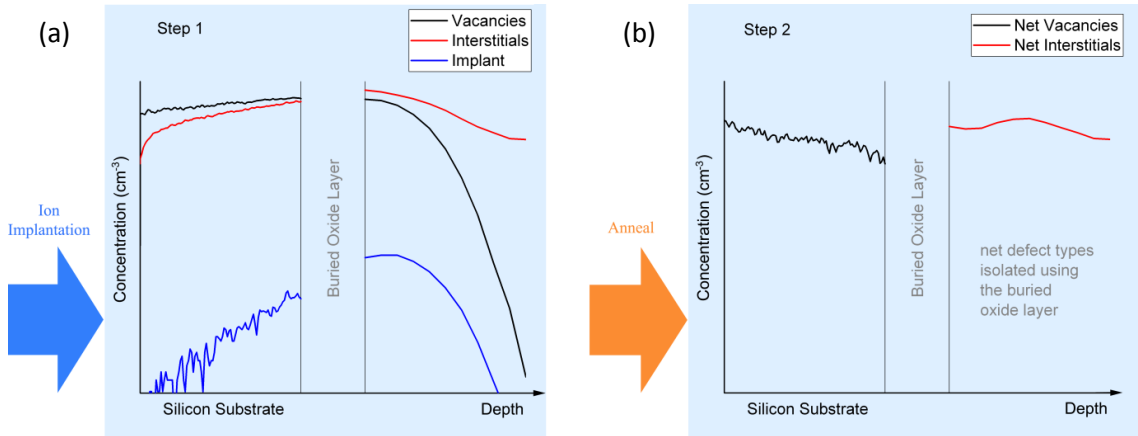


Figure 3.1 Two step process for the creation of a vacancy rich region in an SOI wafer using high energy ion implantation. (a): In step 1, the high energy ion implantation process produces a concentration of both Vacancy (black) and Silicon Interstitial (red) defects significantly in excess of the concentration of implanted Silicon Ions (blue) while ensuring the implant and corresponding damage extend beyond the buried oxide layer of the SOI wafer. (b): In step 2, a post implantation thermal anneal allows repair of implantation damage through the local recombination of vacancies, interstitials and ions. The buried oxide layer acts as a barrier, isolating defects on either side, resulting in the production of a region with a net concentration of vacancies above the oxide layer and a region with a net concentration of vacancies below. This Figure is illustrative of process. Concentrations achievable are a function of implanted ion fluence.

Implanted silicon ions can be seen in blue extending across the uppermost device layer and beyond the buried oxide layer into the handling layer below. Concentrations of vacancies and silicon interstitial resulting from this implant can be seen in black and red respectively. Concentrations of both are shown to be present above and below the buried oxide layer. Vacancy and interstitial defects are produced in concentrations significantly greater than the concentration of silicon ions implanted as a result of the cascading nature of the damage interactions and the large amounts of energy within each implanted ion. A spatial separation between vacancy and interstitial in the direction of the implant can also be noted, resulting from the forward momentum of the implanted ion.

Step 2 involves the use of a rapid thermal annealing process. Without annealing device layer morphology would generally display high levels of lattice disorder alongside concentrations of both silicon interstitials and vacancy defects. Thus thermal energy is applied to the target substrate post implantation allowing a reordering of the crystalline structure - through local recombination of vacancy, interstitial and implanted ion - and the reactivation of any dopant present. The results of this process can be seen in Figure 3.1(b) where annealing has allowed such a recombination to occur. With the buried oxide layer acting as a physical barrier to defect migration during this annealing process, a region containing a net concentration of vacancy defects is found above the oxide layer as a result of the spatial separation identified in Figure 3.1(a). A corresponding region rich in interstitial defects is found below.

3.3.2 Bulk silicon

For bulk silicon materials – including silicon thin films – no defect isolating oxide layer is present with the material structure. In such a case, local recombination of defects can be expected to produce a vacancy neutral sample if the approach outlined for SOI is applied without modification.

For effective use on bulk silicon materials, the implant energy used must be sufficient to allow penetration of the implanted ions beyond the entire sample thickness; ejecting concentrations of implanted ions and produced interstitials from the back surface of the sample itself. Such an approach can be seen in Figure 3.2. Figure 3.2(a) reveals relative concentrations of implanted silicon ions shown in blue alongside concentrations of vacancy (black) and silicon interstitial (red) defects where implant energy is sufficient to allow the implant to penetrate the entire thickness of the targeted silicon substrate. When compared with the implant into SOI as per Figure 3.1(a), it can be seen that a significant concentration of implanted ions and interstitials have been lost from the rear of the sample itself.

The remainder of the process involves a post implant annealing step as detailed in 4.2.1 allowing local recombination of defects alongside the repair of the crystalline lattice and re-activation of any dopant present. As can be seen in Figure 3.2(b), process simulation predicts a net vacancy defect concentration extending throughout the entire bulk material sample. This can be compared to the region of net vacancy defects created within the active device layer for an SOI wafer.

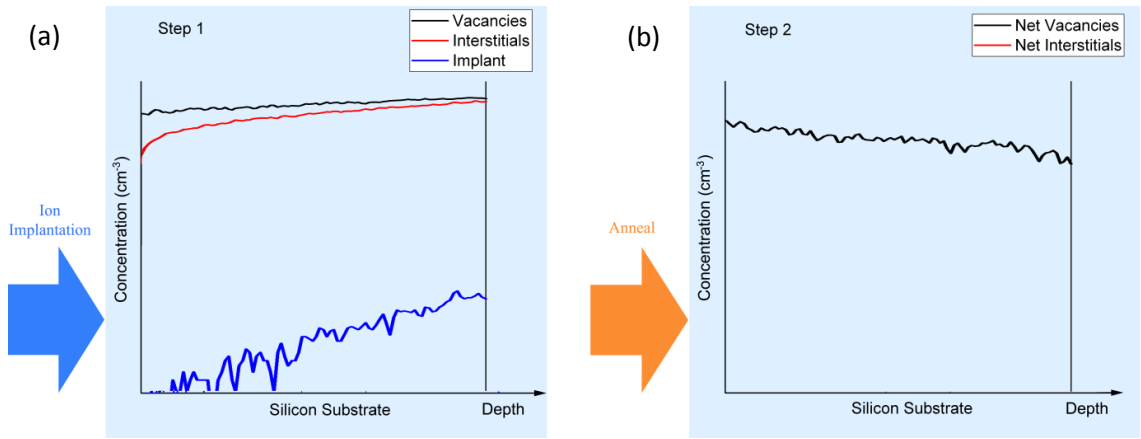


Figure 3.2 Two step process for the creation of a vacancy rich region in a bulk Silicon sample using high energy ion implantation. (a): In step 1, the high energy ion implantation process produces a concentration of both Vacancy (black) and Silicon Interstitial (red) defects significantly in excess of the concentration of implanted silicon ions (blue). The selected implant energy ensures the implant and corresponding damage extend beyond the thickness of the silicon sample itself. (b): In step 2, a post implantation thermal anneal allows repair of implantation damage through the local recombination of vacancies and interstitials. A net concentration of vacancies is left extending across the sample. This Figure is illustrative of process. Concentrations achievable are a function of implanted ion fluence.

3.4 High energy ion implantation

For all samples, high energy ion implantation was undertaken at the University of Surrey Ion Beam Centre. A purpose built High Voltage Europa 2 MV Van de Graaff high energy implanter was used to accelerate a beam of $^{28}\text{Si}^+$ ions at target substrates at room temperature mounted using a standard tilt of 7° . Si ions are acquired using a hot Penning ion source running SiF_4 source gas [101]. Implant parameters are designed using TCAD simulation before samples and parameters are then sent to University of Surrey for manufacture. For all samples, an ion beam energy of 2 MeV – maximum possible at the time of experiments – was combined with a fluence of 8×10^{15} ions/cm².

3.5 Rapid Thermal Annealing

Following high energy self-implantation, a process of rapid thermal annealing (RTA) is required to complete the defect engineering process.

For all samples presented in this work, RTA was undertaken on a Bede D1 x-ray diffractometer (XRD) equipped with an Anton Paar TCU 200 Temperature Control Unit and an Anton Paar DHS 1100 Domed Hot Stage heating attachment. Collective operating temperature range is from ambient to 1100°C

Details of the fitted DHS 1100 heating attachment are shown in Figure 3.3 (a) showing both heater plate and sample retaining clips. Annealing is undertaken with samples isolated from the environment under a graphite dome as shown in Figure 3.3 (b).

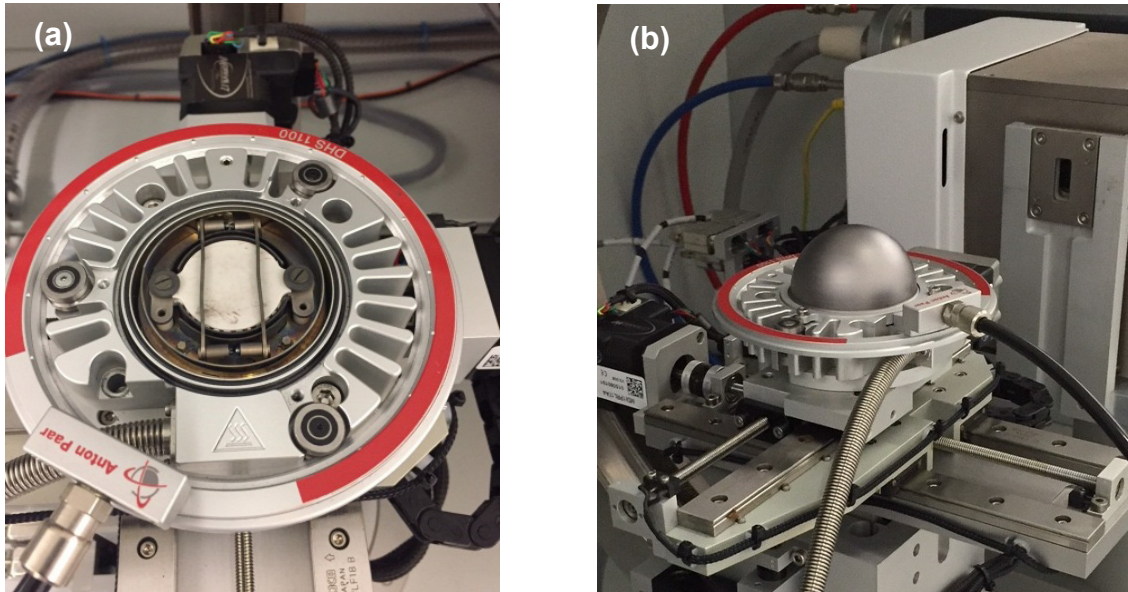


Figure 3.3 (a) Anton Paar DHS 1100 Domed Hot Stage sample heating attachment, and (b) Anton Paar DHS 1100 fitted with graphite dome and attached air lines ready for sample RTA process

Prior to commencing an RTA process, the sample is first placed on an aluminium nitride heater plate fitted centrally within the DHS 1100 before being secured with two retaining clips. This heater plate and retaining clips are designed to ensure a highly uniform temperature distribution. A graphite dome is then placed over the top of the sample and stage before being secured with 3 cap screw fasteners. Once secured, a flow of compressed air is established until the “no air cooling” warning light on the TCU 200 temperature control unit is extinguished; representing a system ready condition. The targeted annealing temperature set point is then entered into the TCU 200 via a Eurotherm 2604 controller. The Eurotherm 2604 is a high precision, high stability process controller offering accuracy of $\pm 0.1\%$ [102]. With the heater activated via the TCU 200 front panel an automatic ramp up process begins with TCU 200 and DHS 1100 working in closed loop mode. Once set point temperature is achieved, this closed loop system precisely holds this RTA temperature until desired RTA duration is reached. The heater is then turned off and the system begins a cooling process back to room temperature. This procedure and apparatus offers high levels of repeatability combined with reliable RTA temperature control and measurement.

3.6 Positron Annihilation Spectroscopy

The study of vacancies introduced to a substrate during the defect engineering process is of significant value but presents challenges given their atomistic scale. The use of positron annihilation spectroscopy offers one solution, allowing depth dependent probing of lattice vacancies to be undertaken using a varying positron implantation energy. The introduction of a positron to the sample results in an annihilation with an electron; producing a pair of gamma rays and the characteristic 511 keV emission of this positron-electron interaction [103]. Introducing a large number of positrons and evaluating the Doppler broadening of the spectrum enables an understanding of vacancy defects within the sample itself to be understood. When plotted as a function of counts versus energy the Doppler broadening reveals both a shape (S) and wing (W) parameter as shown in Figure 3.4. While the W parameter signifies core electron structure, the S parameter is sensitive to open volume defects. With $S_{\text{defects}} > S_{\text{no defects}}$, a comparison of the S parameter for a given sample with the S parameter produced by a defect free control sample can indicate the presence of vacancy defects with the sample under investigation. Comparative evaluation of relative vacancy defect concentrations across multiple samples can also be undertaken by normalising against a defect free control sample.

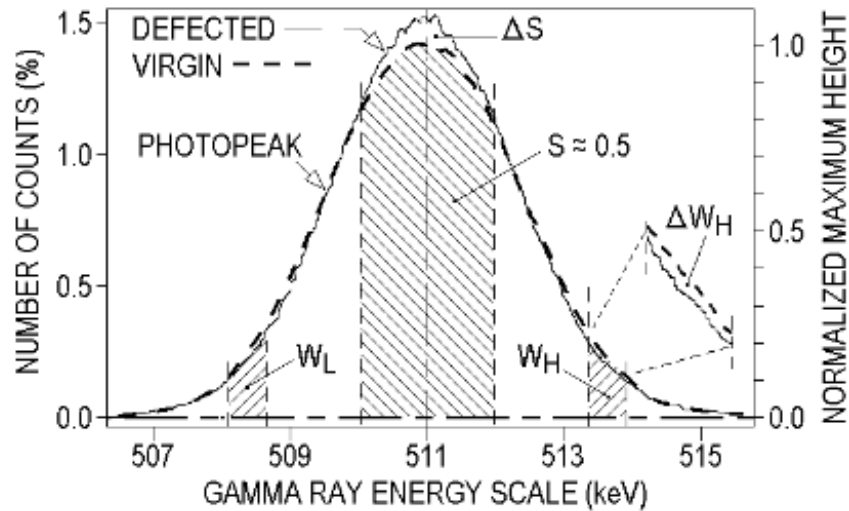


Figure 3.4 Plot of counts versus gamma ray energy resulting from positron annihilation of a sample with vacancy defects and a defect free control sample. The increased S parameter as a result of vacancy defects in the non-virgin sample can be clearly seen [103]

Positron annihilation spectroscopy was undertaken on samples for this work through collaboration with the Reactor Institute of Technische Universiteit Delft. A range of

samples from a silicon-on-insulator wafer were produced using a defect engineering process with constant implant parameters coupled to varying RTA temperatures. These samples were then probed across their device layer using a Variable Energy Positron beam with a Na-22 source using a Doppler broadening technique. Returned S parameters were evaluated against the S parameter returned for an un-implanted, virgin control sample using VEPFIT.

3.7 Scanning Electron Microscope

Investigation of the surface morphology of free standing, thin-film c-Si control samples was undertaken through scanning electron microscopy (SEM). SEM was undertaken at Heriot-Watt University in the School of Engineering and Physical Science Focused Ion Beam facility using an FEI Quanta 3D FEG high resolution scanning electron microscope equipped with an Everhart-Thornley detector. Imaging was undertaken using a magnification of 50,000x and an acceleration voltage of 5kV – values determined through investigation to provide best images of sample surface.

3.8 Resistivity

For many applications, the electrical resistivity of a sample represents a fundamental property of significant interest. In addition to thermoelectric materials, accurate characterisation of metals, semiconductors and insulators requires knowledge of this value.

In the general case, the resistivity (ρ) of an isotropic material can be expressed as the ratio of an applied electric field (E) and the corresponding current density (J) induced by this field thus:

$$\rho = \frac{E}{J} \quad (3.1)$$

With electric field expressed in units of Vcm^{-1} and current density in units of Acm^{-2} , resistivity of a sample is given as Ωcm and represents an intrinsic material property. Resistivity is closely related to the more commonly understood value of resistance through the equation:

$$R = \rho \frac{l}{A} \quad (3.2)$$

Resistance is seen to be a bulk geometric value for the specific sample under investigation, allowing practical measurement through the ratio of voltage U and current I . To transform values of resistance to the material property resistivity, or vice versa, accurate dimensional information for length, l and area, A of the sample itself must be known.

The common approach to obtaining sample resistance typically involves the use of a readily available ohmmeter, where two probes are placed in contact with the sample as seen in Figure 3.5. However such an approach can introduce errors as a result of contact resistance. These contact resistances are in series with the sample resistance resulting in a total value being obtained that represents the sum of these sample and contact resistances rather than that of the sample alone.

A solution to this challenge, mitigating contact resistance effect was first applied to semiconductor materials in 1954 by Valdes [104] and later adopted by ASTM as a procedure for reference measurements [105]. This approach proposed the use of 4 probes for the measurement process. Using two separate pairs of evenly spaced probes aligned on a single plane, the value obtained for resistance can be taken as representing the sample; providing current is passed through the outermost pair, voltage is obtained from the innermost and assuming infinite voltmeter probe impedance. This configuration is shown in Figure 3.6.

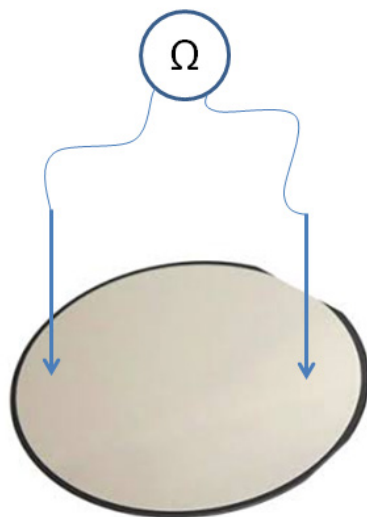


Figure 3.5 Typical resistance measurement using an ohmmeter and two contact probes

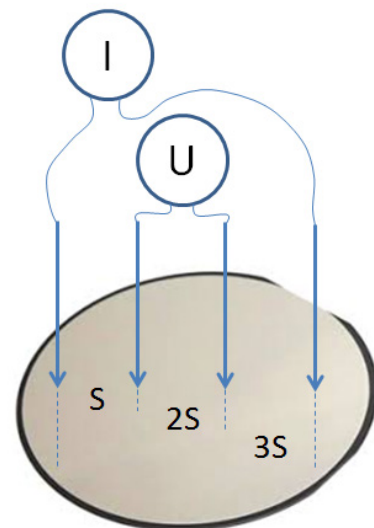


Figure 3.6 4 probe resistance measurement technique using a current source, a voltmeter and four contact probes with even spacing, S

While straightforward, this approach presents some restrictions on relative probe spacing and sample size if complexity via correction factors is to be avoided [106]. Probes must be placed a minimum distance from the edge of the sample; for example ~ 4 times the probe spacing in the case of a large sample with probes near a single non-conducting edge and ~ 20 times the probe spacing if placed centrally inside a circular sample. Sensitivity to errors introduced by probe placement can be understood by investigating these correction factors. In all cases the greatest probe placement related error condition is seen to occur where probes are placed at the edge of a sample. Results obtained under such experimental conditions will be a factor of 2 greater than the actual sample value if no correction is applied.

In addition to probe position, material thickness is also an important consideration when seeking to obtain accurate values. In this case the correction factor applied as a result of the ratio of thickness, t to probe spacing, s can be given as:

$$F = \frac{\ln 2}{\ln \left[\left(\sinh \frac{t}{s} \right) / \left(\sinh \frac{t}{2s} \right) \right]} \quad (3.3)$$

Evaluating this equation reveals an additional challenge. This correction factor returns two functions with different limit conditions. Where $\frac{t}{s} < 0.2$, $F = 1$, while for $\frac{t}{s} > 4$, $F = 2 \ln 2 \left(\frac{s}{t} \right)$

3.8.1 *van der Pauw method for thin film resistivity measurements*

By exploiting these correction factors, a method of significant value for those working on thin film materials was proposed by van der Pauw [107]. This approach enables resistivity measurements to be readily undertaken on a material of arbitrary shape using a 4 probe method providing certain conditions are met. The material under investigation must be free of geometric holes, sample thickness must be less than $1/5^{\text{th}}$ of probe spacing while the probes must be placed at the edge of the sample and small.

In practice, this method allows straightforward measurement of resistivity on many samples without a need for complex preparation or special manufacture using the equation:

$$\exp \left(-\frac{\pi t}{\rho} R_{AB,CD} \right) + \exp \left(-\frac{\pi t}{\rho} R_{BC,DA} \right) = 1 \quad (3.4)$$

Where $R_{AB,CD}$ and $R_{BC,DA}$ represent a pair of resistance measurements with current (I) applied to the first contact pair and potential difference (U) measured at the second contact pair as given by:

$$R_{AB,CD} = \frac{U_{CD}}{I_{AB}} \quad (3.5)$$

$$R_{BC,DA} = \frac{U_{DA}}{I_{BC}} \quad (3.6)$$

In the case of a symmetric sample, $R_{AB,CD} = R_{BC,DA}$ and a single measurement is sufficient. Resistivity can then be found using:

$$\rho = \frac{\pi t}{\ln 2} R_{AB,CD} \quad (3.7)$$

Where sample symmetry is not found, two sets of measurements must be obtained and resistivity calculated using:

$$\rho = \frac{\pi t}{\ln 2} \frac{R_{AB,CD} + R_{BC,DA}}{2} f \quad (3.8)$$

where f is a symmetry factor related only to the ratio of $\frac{R_{AB,CD}}{R_{BC,DA}}$ and expressed thus:

$$\cosh \left[\frac{(R_{AB,CD}/R_{BC,DA}) - 1}{(R_{AB,CD}/R_{BC,DA}) + 1} \frac{\ln 2}{f} \right] = \frac{1}{2} \exp \frac{\ln 2}{f} \quad (3.9)$$

Values for f can be readily obtained from graph as per the original work [107] or from tables as per [108].

For any pairing, improved accuracy can be obtained by measuring the related reciprocal values and substituting mean values of Resistance into the relevant equations. Thus:

$$\overline{R_{AB,CD}} = \frac{R_{AB,CD} + R_{BA,DC} + R_{CD,AB} + R_{DC,BA}}{4} \quad (3.10)$$

$$\overline{R_{BC,DA}} = \frac{R_{BC,DA} + R_{CB,AD} + R_{DA,BC} + R_{AD,CB}}{4} \quad (3.11)$$

and

$$\rho = \frac{\pi t}{\ln 2} \frac{\overline{R_{AB,CD}} + \overline{R_{BC,DA}}}{2} f \quad (3.12)$$

3.8.2 Methodology

Resistivity measurements are undertaken using a Wentworth Laboratories 907 4” Analytical Probe Station featuring a Bausch & Lomb microscope objective and 4 spring tipped gold contact probe arms installed on 3-axis micro-adjusters with magnetic bases. These micro-adjusters allow precise control of probe position on X, Y and Z planes while spring contact tips ensure even and consistent contact pressure is obtained for each probe. Current is provided via a Keithley 224 Programmable Current Source, while potential difference is measured using a Keithley 195A Digital Multimeter.

Probes are placed in 4 positions around the edge of the sample using a combination of optics and 3-axis microadjusters. A typical arrangement for measurement of resistivity using van der Pauw method is shown in Figure 3.7 with associated labelling of each contact also given. Note position of typical probe locations labelled A, B, C and D at the edge of device layer under investigation. Placement should be made as close to the proximity of the physical sample edge as possible to minimise measurement error.

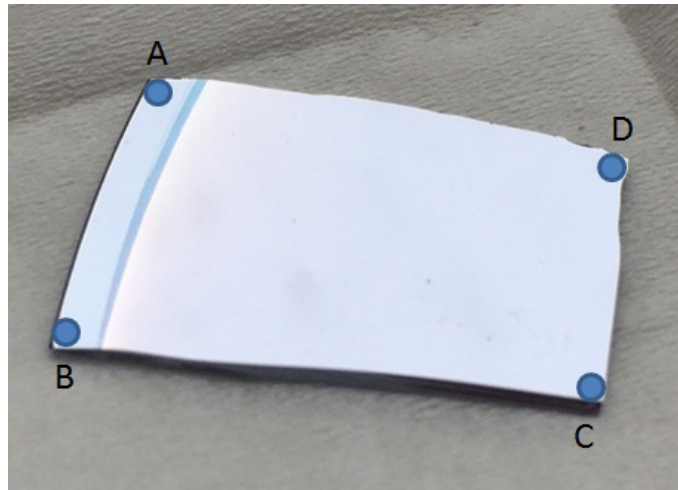


Figure 3.7 Typical probe position and associated labelling for measurement of resistivity using van der Pauw method on an SOI sample. The sample shown is from the edge of a larger Silicon-On-Insulator type wafer.

A series of measurements is undertaken in accordance with Table 3.1 where current source is attached to one probe pairing and potential difference measured across the second pairing. Mean values for $\overline{R_{AB,CD}}$ and $\overline{R_{BC,DA}}$ are then calculated using equations (10) and (11) respectively. A symmetry factor is then derived from tables as per [108] using the ratio of mean resistance measurements $\frac{\overline{R_{AB,CD}}}{\overline{R_{BC,DA}}}$ allowing a resistivity value to be obtained via equation (12).

Table 3.1 Measured resistance value and corresponding current and multimeter connection pairs undertaken using van der Pauw method for calculation of resistivity.

	Measured Resistance Value	Keithley 224 Current Source Connection	Keithley 195A Digital Multimeter Connection
$\overline{R_{AB,CD}}$	$R_{AB,CD}$	A-B	C-D
	$R_{BA,DC}$	B-A	D-C
	$R_{CD,AB}$	C-D	A-B
	$R_{DC,BA}$	D-C	B-A
$\overline{R_{AC,BD}}$	$R_{BC,DA}$	B-C	D-A
	$R_{CB,AD}$	C-B	A-D
	$R_{DA,BC}$	D-A	B-C
	$R_{AD,CB}$	A-D	C-B

3.8.3 Equipment calibration

Both the Keithley 195A Digital Multimeter (DMM) and the Keithley 224 Programmable Current Source offer straightforward, accurate user calibration. Calibration procedures as per manufacturer instructions were undertaken and are summarised here.

Table 3.2 Calibration steps and settings for Keithley 195A Digital Multimeter

Calibration Step	Range to be Calibrated	Calibration Voltage	Calibration Programme Parameter
1	20mV	19.0000mV	19.0000 -3
2	200mV	190.000mV	190.000 -3
3	2V	1.90000mV	1.90000 +0
4	29V	19.0000V	19.0000 +0
5	200V	190.000V	190.000 +0

The Keithley 195A offers 5 ½ digit resolution and a front panel calibration feature allowing calibration to be readily undertaken with suitable test equipment. Following a 2 hr warm up period, a Fluke 5500a multi-product calibrator was used to calibrate a range of DC voltage measurements from 19 mV up to 200 V in line with calibration parameters set out in the product manual and shown in Table 3.2. Accuracy once calibrated is expected to be +/- 0.005%

Calibration of the Keithley 224 Programmable Current Source is undertaken by internal instrument adjustment following a 1hr minimum warm up period in conjunction with a set of resistors and the calibrated Keithley 195A DMM. The basic procedure involves the placing of a shunt resistor of specified value across the output of the Model 224 before setting a current value. The corresponding voltage across this shunt resistor is

then measured and compared to a calculated target voltage obtained by multiplying shunt resistor value and current. For example a shunt resistance of 1 k Ω combined with a Model 224 output of 1.9mA would result in a calculated target voltage for calibration of 1.9V. Where a difference is noted, adjustment is made at the relevant internal adjustment point until allowable specification is obtained.

Internal adjustment points are revealed by removal of the instrument top cover. Adjustment is made by inserting a small screwdriver through each hole and rotating the relevant potentiometer until the desired value is obtained. A range of test shunt resistors used for calibration allows straightforward calibration of all ranges to be achieved by a competent user.

Results of the calibration procedure, including shunt resistors used along with relevant adjustment points are given below.

2mA range calibration

Specified shunt $R = 1\text{k}\Omega \pm 0.1\%$, Actual shunt $R = 0.999\text{k}\Omega$

Range = 1.9E-3A, Compliance = 30V

Target $V = 1.9\text{E-}3\text{A} \times 0.999\text{k}\Omega = 1.8981\text{V} \pm 300\text{ppm}$; Achieved via R303

Range = -1.9E-3A, Compliance = 30V

Target $V = -1.9\text{E-}3\text{A} \times 0.999\text{k}\Omega = -1.8981\text{V} \pm 300\text{ppm}$; Achieved via R318

100mA range calibration

Specified shunt $R = 10\Omega \pm 0.1\%$, Actual shunt $R = 10\Omega$

Range = 100E-3A, Compliance = 30V

Target $V = 100\text{E-}3\text{A} \times 10\Omega = 1\text{V} \pm 750\text{ppm}$; Achieved via R387

20mA range calibration

Specified shunt $R = 100\Omega \pm 0.1\%$, Actual shunt $R = 100.1\Omega$

Range = 19E-3A, Compliance = 30V

Target $V = 19\text{E-}3\text{A} \times 100.1\Omega = 1.9019\text{V} \pm 300\text{ppm}$; Achieved via R387

200 μ A range calibration

Specified shunt $R = 100\text{k}\Omega \pm 0.02\%$, Actual shunt $R = 100.01\text{k}\Omega$

Range = 190E-6A, Compliance = 30V

Target $V = 190\text{E-}6\text{A} \times 100.01\text{k}\Omega = 19.0019\text{V} \pm 250\text{ppm}$; Achieved via R385

20μA range calibration

Specified shunt $R = 100\text{k}\Omega \pm 0.02\%$, Actual shunt $R = 100.01\text{k}\Omega$

Range = $19\text{E-}6\text{A}$, Compliance = 30V

Target $V = 19\text{E-}6\text{A} \times 100.01\text{k}\Omega = 1.90019\text{V} \pm 300\text{ppm}$; Achieved via R384

Calibration in line with manufacture specifications was obtained for all calibration steps. Accuracy is expected to be $\pm 0.1\%$ in the 100 mA range, and $\pm 0.05\%$ across ranges from $10\text{ }\mu\text{A}$ to 10 mA .

3.8.4 Measurement uncertainties as a result of probe position and size

Measurement uncertainties using van der Pauw method are introduced as a direct result of probe size and position. Research into the effects of contact size by Chwang et al suggests that confidence in contacts being defined as “sufficiently small” can be had for contacts as large as 12.5% of sample width [109]. In this condition introduced error was shown to be $\sim 0.25\%$. Probes used in experimental work within this thesis offer a contact width significantly smaller than this 12.5% threshold suggesting uncertainties introduced as a result of contact size can be safely considered insignificant.

An expectation of uncertainties arising due to probe position relative to sample edge can be understood through sensitivity analysis. For a contact placed sub-optimally some distance x from the sample boundary, on a circular sample of diameter D , measurement error can be approximated using the equation:

$$\frac{\Delta\rho}{\rho} = \frac{-x^2}{2D^2 \ln 2} \quad (3.13)$$

The error introduced can be seen to be a function of the ratio arising from the relative distance of the probe from the edge of the sample and the size of the sample itself.

Exact probe position relative to the edge of a given sample when using manual probes can be challenging to accurately determine, however the use of microscope objectives and manual probes with microadjusters enable distances $< 1\text{mm}$ to be repeatedly achieved. To evaluate sensitivity of results obtained to relative probe position, an analysis of a maximum error condition representing a worst case scenario can be undertaken. From equation (13), it can be seen that such a condition will occur for a small sample size combined with large distance of probe from sample boundary. Taking a minimum sample size of 12mm and a maximum probe distance of 1mm from the sample boundary the error introduced is found to remain small. An expected error

of -0.5% is returned, giving a worst case measurement error as a result of probe position of -2% were all 4 probes placed at a similar 1mm distance.

3.9 Charge Carrier Concentration

Determination of charge carrier concentration was undertaken using a Bio-Rad HL5900+ Hall Profiler, allowing validation of samples against manufacturer specifications. This automated system allows for measurement of carrier concentration using the Hall effect through application of van der Pauw method. As with the approach used for measurement of resistivity, 4 probes are placed at the periphery of the sample in a similar configuration to that shown in Figure 3.7. Differing from conventional resistivity measurements however, the voltage across a pair of contacts is measured with and without an applied magnetic field perpendicular to the surface while a current is passed through the remaining contact pairing.

The Hall effect expresses the relationship between this applied magnetic field and the transverse voltage produced as a result of the transverse force exerted on the moving charge carriers. The change in voltage detected with and without the applied magnetic field is the Hall voltage, U_H , allowing the sheet Hall coefficient R_{Hs} to be expressed by:

$$R_{Hs} = \frac{U_H}{BI} \quad (3.14)$$

where I is the current and B the applied magnetic field.

Sheet carrier concentration, N_s can then be calculated using:

$$N_s = \frac{1}{qR_{Hs}} \quad (3.15)$$

where q is the elementary charge of $\sim 1.6 \times 10^{-19}$ C.

Bulk carrier concentration can then be determined by dividing the sheet carrier concentration by the sample thickness.

3.10 Seebeck Coefficient

In addition to electrical resistivity, the material property of Seebeck coefficient represents the second in a pair of electrical characteristics of prime importance for thermoelectric materials. Not only is this coefficient representative of the underlying mechanism by which voltage is produced as a function of an applied temperature

gradient but this term features quadratically in the core equations revealing material thermoelectric performance.

Where a potential difference is produced by a material in the presence of a temperature gradient across it, Seebeck coefficient can be expressed as:

$$U = S(\Delta T) \quad (3.16)$$

Where $\Delta T = (T_2 - T_1) = (T_{hot} - T_{cold})$

While Seebeck coefficient S can be seen to simply and directly describe the ratio of voltage to temperature difference, accurate characterisation provides challenges. These challenges can be categorised as i) seebeck coefficient temperature dependence, ii) experimental challenges relating to accurate measurement of voltage and temperature, and iii) best practice for interpretation of experimental raw data.

An illustration of these challenges can be provided by evaluating results obtained for measurement of Seebeck coefficient using a straightforward approach shown in Figure 3.8. Here a temperature gradient is applied to a suitable material and potential difference produced measured using a voltmeter.

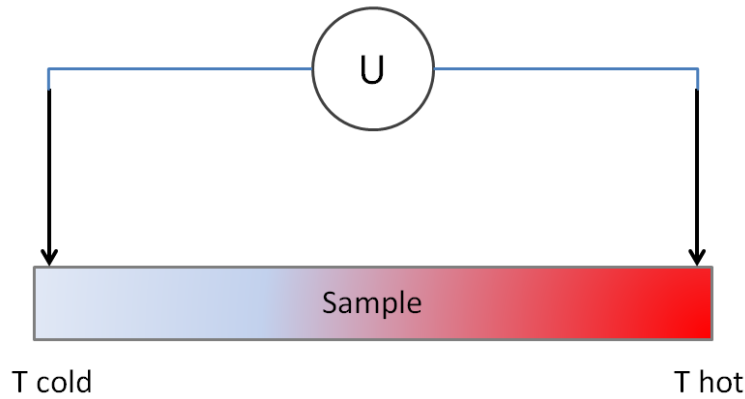


Figure 3.8 A straightforward approach for the measurement of Seebeck coefficient. A temperature gradient is applied across the sample and hot and cold side temperatures monitored while a voltmeter is used to measure corresponding potential difference.

Results obtained for a sample of commercially manufactured Bi_2Te_3 measured using such an approach can be seen in Figure 3.9. Here values are measured for a range of temperature differences from $\sim 5\text{K} - 45\text{K}$. A second axis is plotted in red revealing the hot side temperature of the material for each measurement. The strong temperature dependence of the Seebeck coefficient within the range of temperature measured can be

clearly seen, with values of S increasing with a strongly linear trend in response to a linearly increasing sample temperature. In addition, the sensitivity of single Seebeck measurements to experimental errors is revealed with several returned values showing significant scatter and thus uncertainty. Challenges relating to temperature dependence and experimental sensitivity are further increased by the presence of instrument contributions to overall Seebeck coefficient within values returned.

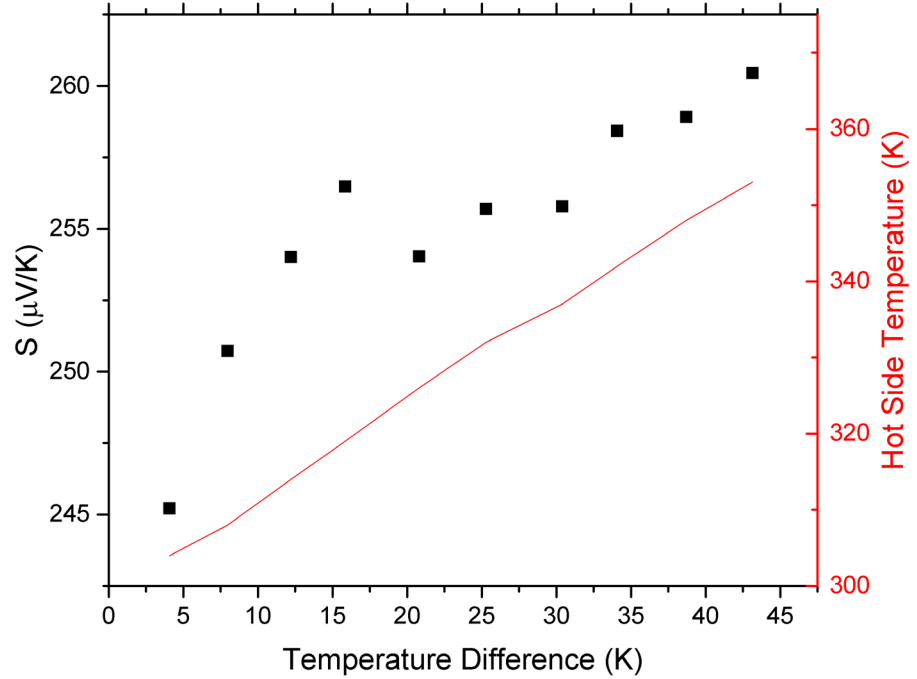


Figure 3.9 Values of Seebeck coefficient as a function of temperature difference for a commercial Bi_2Te_3 sample obtained using a simple measurement approach as shown in Figure 3.8. A second axis showing sample hot side temperature is also included in red revealing the strong temperature dependence of the Seebeck coefficient.

3.10.1 Opportunities for improvements in measurement accuracy

Systems demonstrating improvements in accuracy over the simple approach discussed above are reported in literature [110, 111] [112]. These include improvements to experimental methodology and approach to the use of experimental data. Common to these approaches is the use of a plot of voltage as a function of temperature for a series of measurements as a means of improving accuracy. Seebeck coefficient is obtained from this plot by taking a linear fit and using an equation in the form:

$$U = S(\Delta T) - S_{\text{system}} \quad (3.17)$$

Where slope is taken as representing S at the mean measurement temperature; and the intercept represents the S contribution of the system.

Such a plot is shown in Figure 3.10, where measured values of voltage U are shown as a function of ΔT for the same commercial Bi_2Te_3 sample presented in Figure 3.9. Where Figure 14 reveals significant scatter for the calculation of S individually, Figure 3.10 reveals a strong linear fit with an R^2 value approaching 1. Seebeck coefficient can be taken as $261 \mu\text{V}/\text{K}$, with system contribution $-97 \mu\text{V}$. Challenges around an accurate statement of S should however be noted. While \bar{T} for this measurement range is $\sim 325\text{K}$, sample temperatures vary between 300K and 350K during measurement. Figure 3.9 reveals a strong temperature dependence of S across this range. As a consequence, considerably smaller temperature gradients should be used during measurement if returned values for S are to be truly representative of sample properties at any stated \bar{T} .

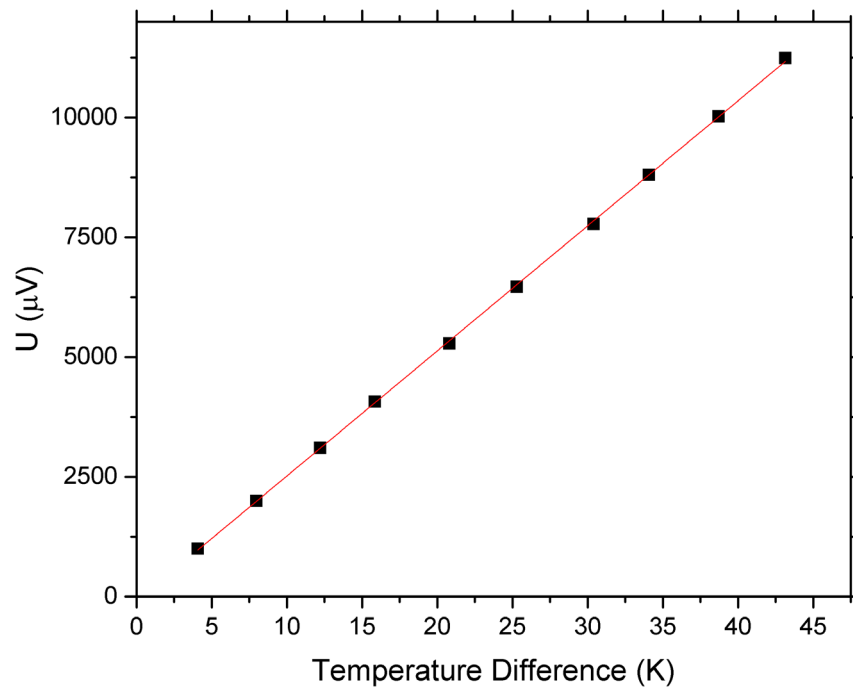


Figure 3.10 Values of voltage as a function of temperature difference for a commercial Bi_2Te_3 sample obtained using a simple measurement approach as shown in Figure 3.8. A linear fit with an R^2 value approaching 1 is shown in red demonstrating significant correlation between value of S obtained from the slope of this line and experimental data itself.

Of significant interest in securing high levels of measurement accuracy is an approach utilised by de Boer [110]; and successfully applied to a 2-D scanning Seebeck coefficient apparatus [112]. Differing from more typical approaches, this method utilises two identical type thermocouples for the measurement of both voltage and temperature across the sample under investigation. Using a switch card, temperature dependent thermocouple voltages are recorded conventionally before a positive and negative voltage is obtained by connecting pairings of positive and negative

thermocouple wires as shown in Figure 3.11. Temperature gradient is initially established before being allowed to decrease as a series of measurements are taken, such that $T_2 > T_1$ represents initial condition while $T_2 \rightarrow T_1$ during experiment.

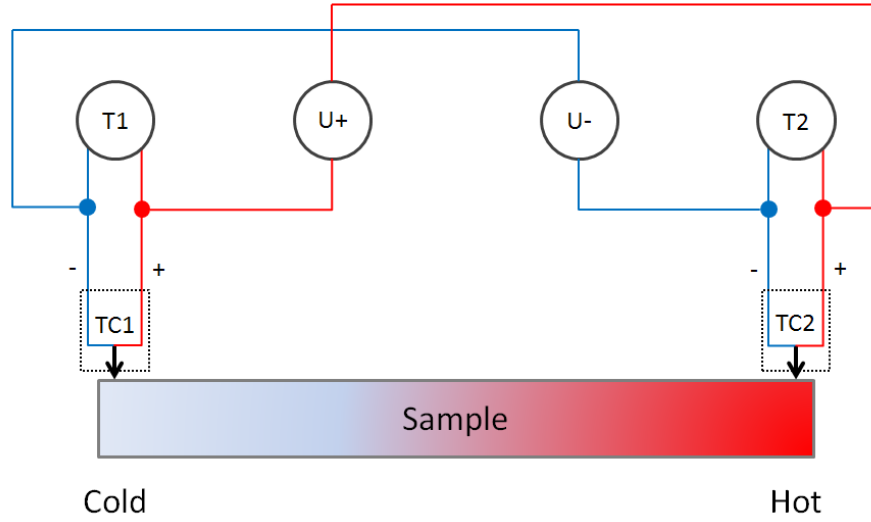


Figure 3.11 Experimental setup and basic wiring configuration for the measurements of Seebeck coefficient using two identical thermocouples in line with approach as per ref [110, 112]. Using a switch card, thermocouples can provide rapid measurement of both temperature and voltage across the sample.

As reported by de Boor, collected experimental data can readily be converted into a value for sample Seebeck coefficient at the mean measurement temperature using:

$$S_1 = -\frac{\partial U_{pos}}{\partial \Delta T} + S_{pos}(\bar{T}) \quad (3.18)$$

$$S_2 = -\frac{\partial U_{neg}}{\partial \Delta T} + S_{neg}(\bar{T}) \quad (3.19)$$

The collection of two voltage measurements at each temperature gradient allows the application of an alternative equation obtained by combining equations (3.18) and (3.19) and then differentiating with respect to a single voltage term. The resultant equation can be given thus:

$$S_{sample}(\bar{T}) = -\frac{S_{TC}(\bar{T})}{1 - \frac{\partial U_{pos}}{\partial U_{neg}}} + S_{neg}(\bar{T}) \quad (3.20)$$

Results obtained using this approach differ from other approaches in that they are a function of $\frac{\partial U_{pos}}{\partial U_{neg}}$. This value can be directly obtained by plotting experimentally obtained values of U_{pos} and U_{neg} and obtaining a linear fit. Values of $S_{TC}(\bar{T})$ and

$S_{neg}(\bar{T})$ can be readily obtained from manufacturer data sheets and literature for the thermocouple type utilised. Using such an approach, the effects of temperature measurement uncertainty applicable in more commonly utilised approaches are reduced. Voltage measurements, and thus the corresponding slope of $\frac{\partial U_{pos}}{\partial U_{neg}}$ are independent of temperature measurement. An influence of temperature accuracy on stated result remains present only in the calculation of mean temperature itself.

3.10.2 Methodology

Measurement of Seebeck coefficient is undertaken using a Linkam Scientific LTS420E-P temperature controlled stage. A centrally located, thermally controllable platform offers both heating and cooling with high temperature stability and is used as a cold side. A second heater stage containing a 25W cartridge heater is controlled using a Lakeshore 325 cryogenic temperature controller operating in closed loop mode through a PT100 RTD surface mounted to the heater block. This block acts as a hot side. Measurement of temperature and seebeck voltages are obtained using 2 k-type grounded thermocouples featuring chromel/alumel elements. Wiring configuration of the thermocouples with respect to obtaining values of Seebeck voltage and temperature are as shown in Figure 3.11. Voltages are acquired using a Keithley 2000 series digital multimeter. Integration of all equipment is provided by LabVIEW, allowing central control of all experimental parameters and logging of environment and stage temperatures alongside thermocouple and seebeck voltages.

Samples are placed with one end on the Linkam stage, and the other on the heater stage ensuring a gap between the two such that the sample under investigation acts as a thermal bridge. Thermocouples are placed towards each end of the sample using 3-axis micro-adjusters with thermocouple bodies orientated vertically. A cold side sample temperature is established before a target hot side temperature is selected and heating applied via the Lakeshore controller. For Seebeck coefficient measurements expressed at 300K a target hot side temperature of 305K is typical. Logging of experimental parameters begins and hot side ramp up begins. Temperature is allowed to rise until reaching target setting before heating power is removed and temperature at the hot stage begins to fall back towards starting value. Logging continues until loss of hot side temperature is complete and measurement ends. Data is then extracted in excel format and measurement points recorded during ramp up discarded. Remaining data is

evaluated with respect to sample temperature and a subset of data selected to provide voltage and temperature readings from both thermocouples over a specific range. Seebeck coefficient is expressed at a mean temperature and data range must be appropriate to ensure maximum and minimum temperature values return targeted temperature. Difference between maximum and minimum temperature must also be sufficiently small so as to reduce effects as a result of the temperature dependence of Seebeck coefficient itself. Where a temperature of 300K is desirable, a sub set of data is typically selected where maximum temperature is 301K and minimum temperature 299K.

A plot of Seebeck voltages logged at each thermocouple, denoted by U_{pos} and U_{neg} , is produced and a slope of the linear fit extracted. Seebeck coefficient for the sample under investigation can then be obtained using equation (3.20) presented previously, where:

$$S_{sample}(\bar{T}) = -\frac{S_{TC}(\bar{T})}{1 - \frac{\partial U_{pos}}{\partial U_{neg}}} + S_{neg}(\bar{T}) \quad (3.21)$$

3.10.3 Evaluation of uncertainties using U_{pos} versus U_{neg} approach

Calculation of $S(\bar{T})$ via equation (3.21) utilises voltage measurements that are completely independent of any temperature measurement. While conventional approaches rely on a plot of U as a function of ΔT , leaving calculated values of $S(\bar{T})$ reliant on good temperature measurement accuracy, the use of a linear fit obtained from a plot of U_{pos} as function of U_{neg} has no such sensitivity. Although errors introduced via inaccurate temperature measurement are thus reduced, they are not removed entirely. Accurate temperature measurement is still required for the calculation of mean temperature, \bar{T} itself.

An evaluation of system temperature measurement accuracy was undertaken by logging temperature at a 300K target temperature. Measurements were taken for a duration of 300s using a sample rate of 16.6 Hz and 0.6 Hz corresponding to 4980 and 180 logged measurement points respectively.

In both cases, temperature was found to be 299.6 K +/- 0.4 K demonstrating an insensitivity of measurement to choice of sample rate. While such accuracy is

acceptable for a statement of mean temperature, it can be considered problematic were such an uncertainty to be utilised in the calculation of a slope using U as a function of ΔT ; especially where a maximum temperature gradient of $\leq 5\text{K}$ is required to minimise effects of material temperature dependence.

While results obtained using equation (3.21) can be achieved without sensitivity to temperature measurement accuracy, equation (3.21) is not entirely free of uncertainty. Values of S for both the thermocouple and the thermocouple negative leg are required if a result is to be obtained. For a K type thermocouple comprising chromel and alumel, such material properties are readily available in literature [113] [114] and manufacturer data sheets. Nonetheless, some discrepancy exists in reported values, introducing uncertainty into accuracy of results. Sensitivity to variation in reported values can be understood by evaluating maximum uncertainties for each term. Uncertainty in $S_{TC}(\bar{T})$ can be taken as $\pm 0.5 \mu\text{V/K}$, while for $S_{neg}(\bar{T})$ a maximum uncertainty of $\pm 1 \mu\text{V/K}$ can be expected. Calculation of results using a commercial Bi_2Te_3 sample with such uncertainties reveals an effect on result of $\sim \pm 1.2\%$ and $\sim \pm 0.4\%$ respectively. With total uncertainty less than 2%, values of S obtained using this approach can be considered to have good accuracy.

3.10.4 Use of pseudo steady-state versus steady-state

Following the approach reported in [110], the measurement of S undertaken in this work utilises a pseudo steady-state condition for each measurement rather than an actual steady-state condition. That is to say that while temperature gradient is dynamic during the measurement series, for each group of measurements – comprising $U_{hot}, U_{cold}, U_{pos}, U_{neg}$ – a fast sample rate allows each intermediate gradient to be taken as static. Such an approach brings considerable benefits, enabling a series of measurement points to be obtained during an experiment where starting (and thus maximum) temperature gradient must be small to avoid effects of material temperature dependence. While benefits of this approach are considerable, a true steady-state method would allow the collection of multiple data points at each gradient step within the series. Despite the considerable experimental challenges faced by a true steady state approach, it is worthwhile nonetheless to evaluate the influence of multiple recorded measurements versus a single measurement on results.

A series of measurements comprising recorded temperatures and sample voltages at 10 steady-state conditions between $\sim 303\text{K}$ and $\sim 355\text{K}$ were recorded. Figure 3.12 shows a histogram of temperatures recorded at the initial $\sim 303\text{K}$ starting temperature. Temperature can be seen to fluctuate between 303K and 302K during measurement while distribution is seen to be stochastic rather than following a normal distribution. A similarly stochastic distribution can be seen in Figure 3.13 (a) and (b), where a histogram of U_1 and U_2 voltages recorded at the same temperature of $\sim 303\text{K}$ is shown. Such a pattern of stochastic rather than normal distribution was found for all recorded data series. Such distributions suggest that multiple measurements taken at the same temperature point are unlikely to yield an improvement in accuracy of result through increased volume of information.

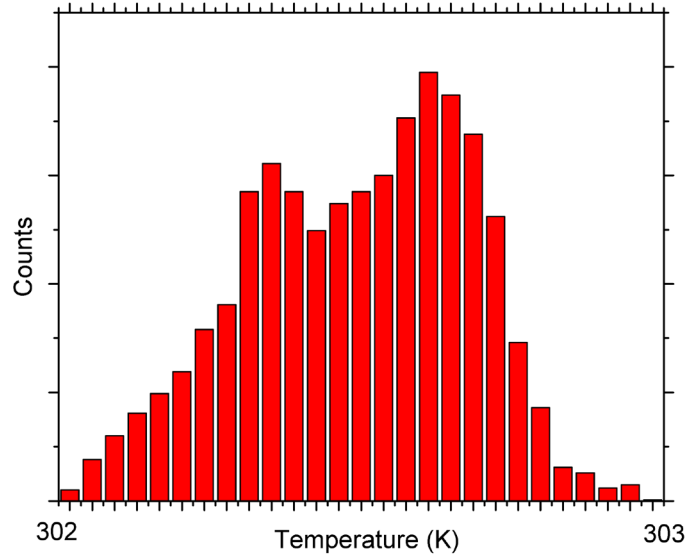


Figure 3.12 Histogram of steady state temperature distribution at $\sim 303\text{K}$

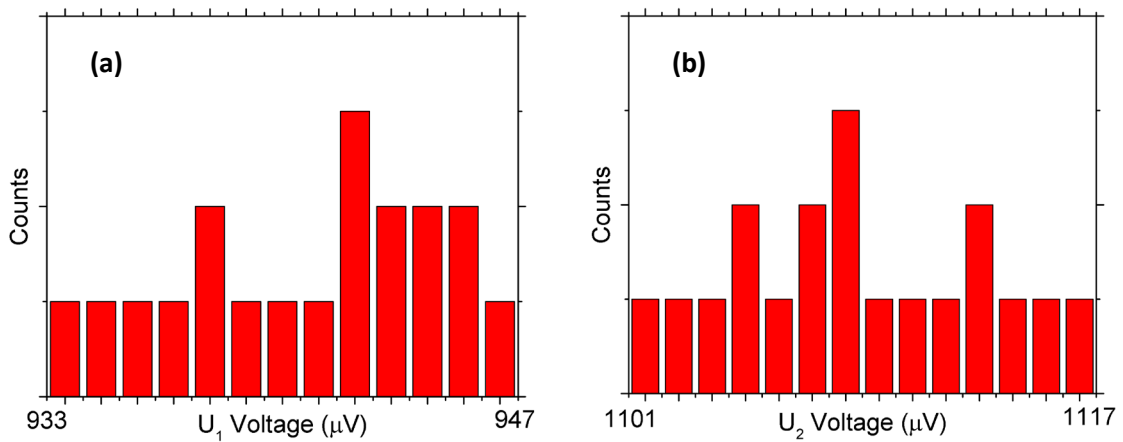


Figure 3.13 Histogram of (a) U_1 voltage and (b) U_2 voltage recorded during steady-state temperature of $\sim 303\text{K}$ shown in Figure 3.12

In order to test this hypothesis, plots of U_2 vs U_1 were produced from the recorded data using three conditions: (i) mean values of U_2 and U_1 using all available data points for each series, (ii) only the first data point for U_2 and U_1 is selected from each series representing the pseudo steady-state approach, and (iii) a random number generator was used to select a data point for U_2 and U_1 from each series. Results can be seen in Table 3.3 where slope of U_2/U_1 obtained from each plot is shown alongside relevant calculated values of S .

Table 3.3 Slope of U_2/U_1 and associated Seebeck coefficient for a commercial Bi_2Te_3 sample calculated using the mean value, the first value and a random number generator selected value from each available data set.

	Method		
	Mean	First Point from Set	RNG Selected
Slope of U_2/U_1	1.17829	1.1772	1.17758
Seebeck Coefficient	-242.354 $\mu\text{V/K}$	-243.734 $\mu\text{V/K}$	-243.251 $\mu\text{V/K}$

In line with expectations following evaluation of temperature and voltage histograms, no significant difference is noted between each result. Variation in S found to be +/- 0.3%. Such an outcome is suggestive that no benefit is to be achieved through the addition of multiple data points were the approach changed to a true steady-state method. The approach based on the pseudo steady-state utilised in this work can be expected to yield statistically identical results without incurring the penalty of additional experimental complexity.

3.11 Thermal Conductivity

The application of vacancy defect engineering to silicon samples in this work specifically targets reductions in thermal transport. Measurement of this parameter must be undertaken if relative changes in performance are to be evaluated. Initial measurements were undertaken by a commercial vendor using an Advance Riko TCN-2 ω thermal conductivity meter. This meter offers ready measurement of thermal conductivity at room temperature using a 2-omega approach. This approach applies periodic heating to a metal film deposited on the surface of the sample as a means of determining sample thermal conductivity using a one dimensional heat flow model. Use of this vendor offered consistency of approach with the proof of principle study undertaken on 100 nm thick SOI wafer [14]. These advantages of experimental

continuity and ready measurement were however offset by limitations applicable to samples featured in this work. Firstly, measurement using this apparatus was destructive as a result of required surface deposition. A significant concern given limited availability of samples. Secondly, the one dimensional heat flow model underpinning this approach requires that heat completely arrive at the bottom substrate during measurement. Sample thicknesses approaching $2\text{ }\mu\text{m}$ combined with potentially high levels of thermal conductivity in samples annealed at high temperatures introduced significant uncertainty in this respect. Heat was potentially likely to dissipate throughout the sample. To address these challenges, an analytical model was developed and reported during this work allowing an alternative method of measurement. This approach offered non-destructive, non-contact measurement of sample thermal conductivity building on an existing approach using micro-Raman spectroscopy. Accuracy was improved by a factor of 2 over existing models, while an extension was developed allowing i) evaluation of substrate influence on experimentally measured values, and ii) extraction of estimates for sample-only values where an influence was identified. This work is presented in Chapter 4, allowing a fuller discussion to be provided.

Chapter 4: Development of a model for non-contact, non-destructive measurement of thermal conductivity

4.1 Background

The measurement of thermal conductivity is crucial for research undertaken during this work. Samples produced following a vacancy defect engineering approach require evaluation via this property as a means of determining success. Accurate measurement using existing approaches however presented challenges. Conventional approaches required costly equipment and/or significant experimental complexity and were often destructive in nature, while further challenges were presented from alternative approaches returning values which were otherwise indirectly inferred. Although an innovative alternative had been previously reported, it lacked sufficient accuracy for the samples under investigation. In all cases, such challenges were compounded by limitations in obtaining a value of thermal conductivity for a sample alone where a substrate or supporting structure was present. For many samples produced during this work - and indeed that of others - no suitable approach was available to accurately and directly obtain an estimation of thermal conductivity.

As a consequence, an analytical model was developed and reported to address these challenges, allowing thermal conductivity to be measured free of existing limitations via a straightforward, non-destructive approach using micro-Raman spectroscopy [89]. Results obtained experimentally were compared to those obtained using a complimentary technique and an improved accuracy over existing micro-Raman based approaches was demonstrated. In addition to this significant improvement in accuracy, this new model enables the effect of any substrate or supporting structure on measured values of thermal conductivity to be quantified. Importantly, estimations of thermal conductivity for the sample itself are now possible where such an influence is determined. Current estimations determining the threshold of substrate influence were shown to be insufficient and the importance of obtaining values of thermal conductivity for the sample itself under such conditions was demonstrated.

This chapter details the underlying work behind this model before discussing its application in obtaining thermal conductivity values presented within Chapter 6 of this thesis.

4.2 Micro-Raman Spectroscopy

Raman spectroscopy, named after its experimental discovery by C.V. Raman in 1928, is a vibrational spectroscopy technique in wide use; particularly in areas of Chemistry where it can be used to identify substance composition, in addition to applications quantifying changes to crystallinity and stress [115-118]. By irradiating a sample with a monochromatic light source, Rayleigh and Raman scattering can be induced and collected. In both cases, this irradiation excites the electrons surrounding a molecule into a virtual state. The inherent instability of this virtual state causes an instantaneous re-radiating of the photon. For Rayleigh scattering – the dominant re-radiation process – this excitation is accompanied by a return of electrons to the ground state and an emitted photon with the same energy, and thus wavelength as the original source. In the case of Raman scattering, emitted photons possess a wavelength different to the incident light. Raman scattering contains two classifications. In the case of Stokes Raman scattering, electrons do not return to this ground state, but instead return to a vibrational level above this ground state. The resulting photon has less energy, and thus a longer wavelength than the original source. For anti-Stokes Raman Scattering, electrons already in a vibrational state are excited to a higher virtual state before returning to the ground state. This produces a photon with greater energy and thus shorter wavelength than both Stokes Raman scattering and the original incident light itself. These scattering types can be seen in Figure 4.1. Raman scattering is a weak process with approximately 10^6 - 10^8 Rayleigh photon scatters occurring to a single Raman scattering.

Raman spectra are represented visually as a function of intensity and wavenumber, with wavenumber given in units of cm^{-1} and expressed as a function of excitation and scattered wavelengths using $\left(\frac{1}{\text{excitation wavelength}} - \frac{1}{\text{scattered wavelength}} \right)$

This approach ensures straightforward comparison between Raman spectra obtained using different laser sources. The returned Raman shift remains constant irrespective of the excitation wavelength used. For example, measurements undertaken on silicon samples using a 488nm and a 785nm laser will return Stokes Raman scattered wavelengths in the range of 500nm and 818nm respectively. Raman shift expressed in terms of wavenumbers for each will however be $\sim 520\text{cm}^{-1}$.

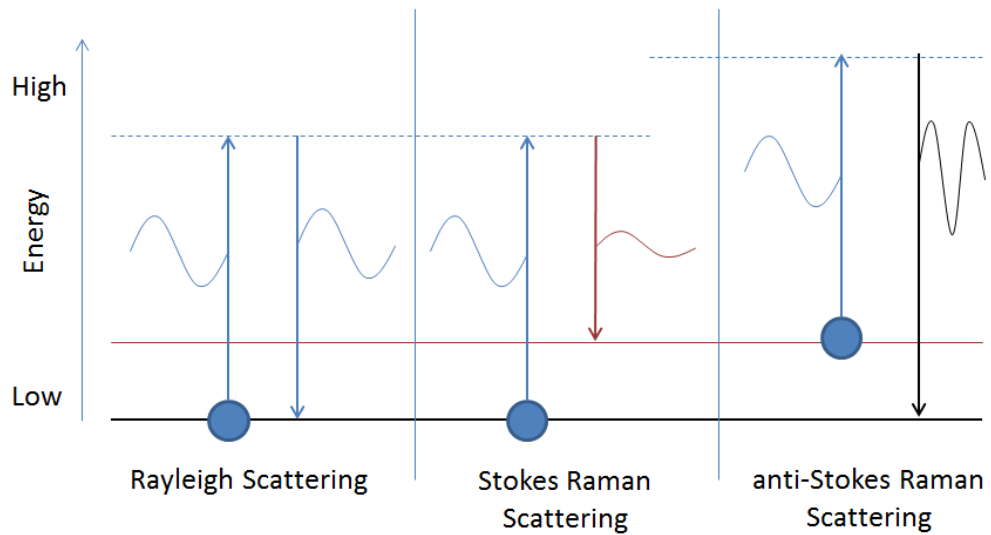


Figure 4.1 Rayleigh, Stokes Raman and anti-Stokes Raman scattering showing an excitation of an electron by an incident light source to a virtual state and subsequent photon emission. For Rayleigh scattering, electrons return to ground state and photon wavelength matches incident light. For Stokes Raman scattering the electron returns to a vibrational state and emitted photon has a longer wavelength. For anti-Stokes Raman scattering, the electron begins in a vibrational state before returning to ground state, resulting in the emission of a photon with a shorter wavelength than the incident light source.

4.3 Thermal Conductivity using micro-Raman Spectroscopy

Micro-Raman spectroscopy has been demonstrated to provide effective non-contact thermometry, drawing on a temperature dependence of the obtained Raman peak shift [118-122]. Such an approach has been enhanced further by the demonstration of non-destructive extraction of thermal conductivity, taking advantage of the localised heating effect of a laser [123-126]. However limitations in the practical application of such measurement techniques remain – particularly for nano-film / thin-film materials and associated microsystems.

Where samples do not meet restrictive dimensional criteria or are in contact with a substrate or supporting structure, difficulties in isolating sample thermal conductivity from what is an experimentally measured apparent thermal conductivity can often be encountered. In many cases a representative solution for the properties of the sample itself cannot be obtained.

An approach to micro-Raman thermal conductivity measurement has been previously presented [127]. This approach requires the sample thickness to be at least an order of magnitude greater than the laser diameter in order to eliminate any substrate effect from measured thermal conductivity creating a practical barrier for many applications using

thinner materials. A solution was offered to this limitation for sub-micrometer samples where sample isolation cannot be assumed [128]. This solution, following an approach by Dryden *et al.*[129], also requires specific sample/substrate conditions to be met. Such conditions treat the sample as a thin coating where ratio of sample thickness to laser spot radius approaches zero providing an equation dominated by substrate thermal conductivity. Such an approach also requires that substrate thermal conductivity be much greater than that of the sample. While alternative equations can be derived via the original work [129, 130] to allow for conditions where i) a sample has high thermal conductivity relative to the substrate or ii) is of sufficient dimension to be considered a thick coating *i.e.* sample thickness more than twice the laser radius; the results obtained by such thin and thick coating approximations can differ significantly even as coating thicknesses converge. This creates uncertainty in approach and a difficulty in achieving solutions for a range of material thicknesses and conditions.

The use of a free standing geometry to remove any substrate effect has been successfully demonstrated on materials including silicon and graphene [125, 126, 131-133]. By suspending a sample over a hole – for the case of samples with no fixed substrate – or removing an area of substrate to produce a free standing section of sample, direct measurement of thermal conductivity via micro-Raman spectroscopy can be undertaken. Although effective in removing the contribution of the substrate to any measured value of thermal conductivity, such approaches present practical restrictions.

Such limitations reduced the opportunities for the measurement of thermal conductivity via a micro-Raman spectroscopy based approach, leaving alternative methods that may compromise samples via metallic deposition and/or require relative complexity in experimental design or analysis [134-138].

In response, a theoretical model addressing these limitations was developed. Firstly, an updated approach allowing a more accurate estimation of thermal conductivity via micro-Raman data is given; and this improved accuracy is further demonstrated experimentally. Secondly, a thermal restriction parameter is developed allowing a numerical solution for sample thermal conductivity itself to be isolated if a substrate or supporting structure influence is present. Limitations based upon relative layer properties and associated effects are avoided.

Using this model, thermal conductivity can be readily and universally obtained for samples where measurement difficulties are presently encountered, while a more

rigorous interrogation can also be undertaken for samples where measurement via a micro-Raman approach remains more straightforward. Results can be obtained even as the ratio of sample thickness to laser radius is varied across a wide range.

Sample thermal conductivity can therefore be directly evaluated for a wide variety of material properties and dimensions via an approach that is both straightforward and non-destructive. The contribution of any substrate or support structure to experimentally measured thermal conductivity can also be understood allowing for the isolation of sample thermal conductivity on dual layer components and systems.

4.4 Analytical Model

4.4.1 *Measurement of thermal conductivity*

The application of micro-Raman thermometry and subsequent extraction of thermal conductivity draws upon the temperature dependence of an obtained Raman peak shift. By varying input laser power - and thus heat flux - a relative peak shift and associated temperature change can be induced and recorded providing sufficient laser power is available to produce a surface temperature rise. Combining these effects allows a Raman measured thermal conductivity to be obtained for both sample and any substrate or supporting material using standard micro-Raman equipment.

Under steady state conditions, an approximately isothermal surface condition can be assumed to occur over the circular laser spot as per Figure 4.2. For such conditions surface temperature T for a circular laser spot of radius a can be derived using:

$$\frac{\partial T}{\partial x} = f(r) = \frac{-Q}{2\pi ak(a^2 - r^2)^{\frac{1}{2}}} \quad \text{where } a \geq r > 0, \quad x = 0. \quad (4.1)$$

Evaluating $f(r)$ gives,

$$T = \frac{Q}{4ak} \quad \text{where initial temperature } T_0 = 0. \quad (4.2)$$

The above equation for T can be found in heat conduction textbooks such as [139] where it is discussed in the context of heat flux in a half space from a circular heat source at the surface. An expansion is provided in section 4.4.2

Rearranging yields:

$$k = \frac{Q}{4aT} \quad (4.3)$$

For a laser beam with Gaussian distribution and beam waist given as w , the total heat flux contained within a circle of any given radius on a plane transverse to the beam can be calculated as [140]

$$Q = P(1 - e^{-2r^2/w^2}) \quad (4.4)$$

Thus, where laser spot radius a equals beam waist, the fraction of absorbed power P within the laser spot is

$$P(1 - e^{-2}) = 0.865 P \quad (4.5)$$

Allowing an equation for thermal conductivity to be written

$$k = \frac{P(1 - e^{-2})}{4aT} \quad (4.6)$$

For many samples, the value of thermal conductivity obtained via equation (4.6) may well represent an overall or apparent value rather than offer a measure of the thermal conductivity of the sample alone. In such cases further analysis is required to establish the impact of any substrate or supporting material so that a representative sample thermal conductivity can be isolated.

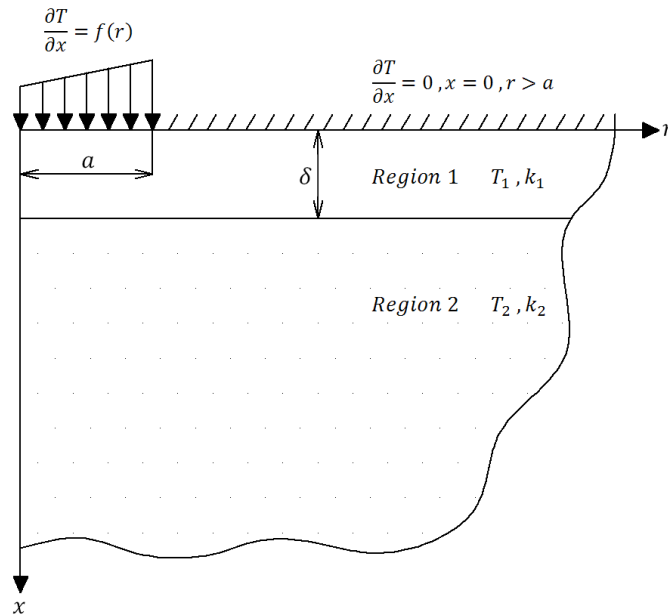


Figure 4.2 Circular heat source of radius a on a half space of radius, r and depth, x

4.4.2 Determination of substrate influence and estimation of sample-only thermal conductivity

The introduction of a heat flux via micro-Raman thermometry can be considered as shown in Figure 4.2 where a circular heat source of radius a acts on a half space of radius r with depth x .

The sample of thickness δ is represented by region 1, where $x > 0$ and any substrate present is represented by region 2, where $x > \delta$.

Under steady state conditions, Laplace equations must be satisfied in both sample and substrate. Therefore:

$$\nabla^2 T_1 = 0 \quad r > 0, \quad 0 < x < \delta \quad (4.7)$$

$$\nabla^2 T_2 = 0 \quad r > 0, \quad x > \delta \quad (4.8)$$

where:

$$\nabla^2 = \frac{\partial^2}{\partial r^2} + \frac{1}{r} \frac{\partial}{\partial r} + \frac{\partial^2}{\partial x^2} \quad (4.9)$$

With continuity of heat flux and temperature at the interface between sample and substrate:

$$T_1 = T_2 \quad r > 0, \quad \delta = x \quad (4.10)$$

$$k_1 \frac{\partial T_1}{\partial x} = k_2 \frac{\partial T_2}{\partial x} \quad r > 0, \quad \delta = x \quad (4.11)$$

Boundary conditions at $x = 0$ can be given as:

$$\frac{\partial T_1}{\partial x} = f(r) \quad a \geq r > 0, \quad x = 0 \quad (4.12)$$

$$\frac{\partial T_1}{\partial x} = 0 \quad r > a, \quad x = 0 \quad (4.13)$$

$$\text{And as } (r^2 + x^2)^{\frac{1}{2}} \rightarrow \infty, \quad T_1 \text{ and } T_2 \rightarrow 0 \quad (4.14)$$

For a laser contact radius with a surface steady state isothermal distribution

$$f(r) = \frac{-Q}{2\pi ak(a^2 - r^2)^{\frac{1}{2}}} \quad (4.15)$$

Therefore

$$\frac{\partial T_1}{\partial x} = f(r) = \frac{-Q}{2\pi ak(a^2 - r^2)^{\frac{1}{2}}} \quad 0 < r \leq a, \quad x = 0. \quad (4.16)$$

Evaluating for a as per [139, 141] and others yields,

$$Q = 4akT \quad (4.17)$$

Such an approach allows the overall thermal resistance, R , of the sample and any substrate present to be expressed.

$$R = \frac{T - T_0}{Q}, \quad \text{thus} \quad (4.18)$$

$$R = \frac{1}{4ak} \quad \text{where initial temperature } T_0 = 0 \quad (4.19)$$

Taking an approach to overall thermal constriction resistance by Negus *et al* [142], a dimensionless thermal restriction parameter for such an isothermal condition can be given as:

$$\psi = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.20)$$

where;

$$I = \left(-2n \frac{\delta}{a} + \left[\frac{1}{2} \sin^{-1}(\tau^{-1}) \right] + \left[(1 - \tau^{-2})^{\frac{1}{2}} \left(\tau - \frac{1}{2\tau} \right) \right] \right) \quad (4.21)$$

$$\tau = \left(n \frac{\delta}{a} + \left[n^2 \left(\frac{\delta}{a} \right)^2 + 1 \right]^{\frac{1}{2}} \right) \quad (4.22)$$

$$\alpha = \frac{\left(1 - \left[\frac{k_1}{k_2}\right]\right)}{\left(1 + \left[\frac{k_1}{k_2}\right]\right)} \quad (4.23)$$

With k_1 sample thermal conductivity and k_2 substrate thermal conductivity. Note a correction to a mistype in the equation as originally presented in reference [25], and also identified by reference [143]

The dimensionless thermal restriction parameter can also be expressed as

$$\psi = k_1 a R, \quad (4.24)$$

yielding

$$\psi = \frac{k_1}{4k_{\text{apparent}}} \quad (4.25)$$

and

$$\frac{k_1}{4k_{\text{apparent}}} = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.26)$$

From the above, a straightforward numerical solution for the thermal conductivity of a sample can be found where laser radius, sample thickness and substrate material properties are known.

4.5 Experimental Validation

In order to evaluate the accuracy of solutions provided by our model, micro-crystalline silicon samples containing two alternative dopant species were obtained and thermal conductivity measured.

These samples were manufactured commercially by Jülich in Germany. A $1 \mu\text{m}$ thick micro-crystalline silicon film was applied onto glass substrates ($\sim 1 \text{ mm}$ thick, $k = 1.025 \text{ W/mK}$) via plasma enhanced chemical vapour deposition using an analogous approach as in reference [144]. P-type samples containing boron were characterised post-manufacture and found to have a resistivity of $0.13 \Omega \text{ cm}$ with a dopant concentration of $\sim 10^{19} \text{ cm}^{-3}$.

N-type samples manufactured with phosphorus were found to have a resistivity of $0.01 \Omega \text{ cm}$ with a corresponding dopant concentration of $\sim 10^{20} \text{ cm}^{-3}$.

Measurements were undertaken utilising a JY Horiba LabRam HR 800 micro-Raman spectroscope located at Dublin City University, Ireland. An argon ion laser with a wavelength of 488 nm, maximum power output of 8 mW and a focused spot size of 1 μm was used throughout.

The position of the Si-Si transverse optical phonon peak as a function of temperature was obtained using a Lakeshore 325 temperature controller in conjunction with a 25 W heater and 2 platinum PT 100 resistance temperature detectors (RTDs) in 4 wire configuration. One RTD provided feedback to the Lakeshore 325 allowing closed loop control of heater power output, while a second RTD provided independent verification of sample temperature. The use of a 4 wire configuration offers high levels of accuracy through an independence of lead wire resistance.

4.5.1 Temperature dependent Raman peak shift

Measurements of the position of the Si-Si transverse optical phonon peak as a function of temperature were undertaken using a low laser power to minimise localised heating effects. Data was recorded for each position and fitted using a Voigt profile. The temperature dependence of this Si-Si transverse optical phonon peak position is shown in Figure 4.3. Peak position is shown to vary $\sim 0.02 \text{ cm}^{-1} \text{ K}^{-1}$, a value in line with temperature dependent peak shift reported elsewhere [118]. Error bars represent the peak position uncertainty returned following fitting of the acquired spectra data.

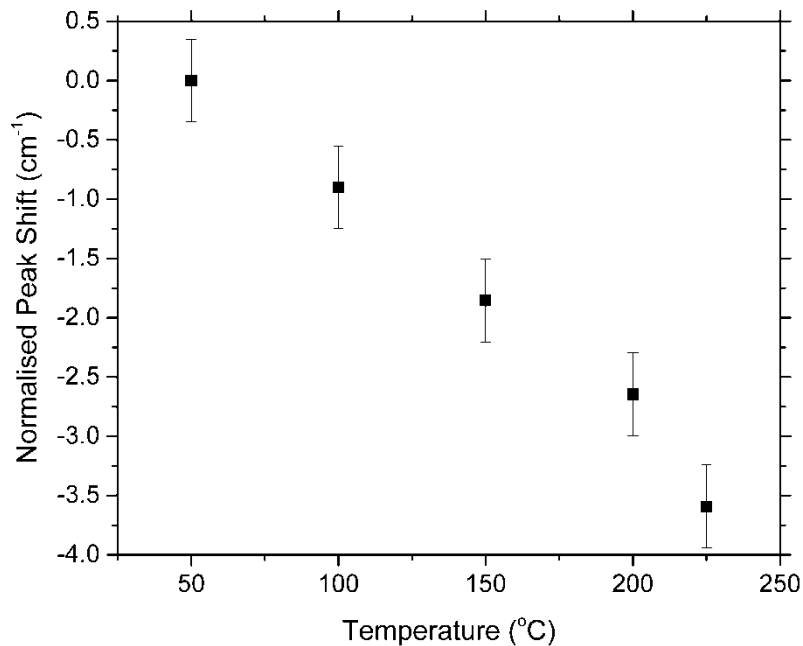


Figure 4.3 Raman peak shift as a function of temperature normalised relative to the peak shift at room temperature.

4.5.2 Flux dependent Raman peak shift

Samples were further measured at fixed (room) temperature using a conventional micro-Raman technique to establish flux dependent Si-Si transverse optical phonon peak shift. Laser flux was varied between 1%, 10%, 25%, 50% and 100% of maximum and Raman peak position recorded for each condition. Data was fitted using a Voigt profile and the normalised Raman peak position plotted. Results are shown in Figure 4.4 and 4.5 where effect of increasing laser flux on peak shift position can be clearly seen. Error bars again represent the uncertainty as to peak position following fitting of the acquired spectra data.

For both samples, input laser power $\leq 25\%$ is found to be insufficient to produce any significant change in the position of the Si-Si transverse optical phonon peak. Peak position remains stable for flux values within this range indicating minimal laser induced heating and associated temperature change. Conversely, laser flux conditions of 50% and 100% are seen to produce a measurable change in Raman peak position allowing application of this model. Under steady state conditions this can be taken to represent an increase in isothermal surface temperature within the laser spot as a result of a laser induced heating effect.

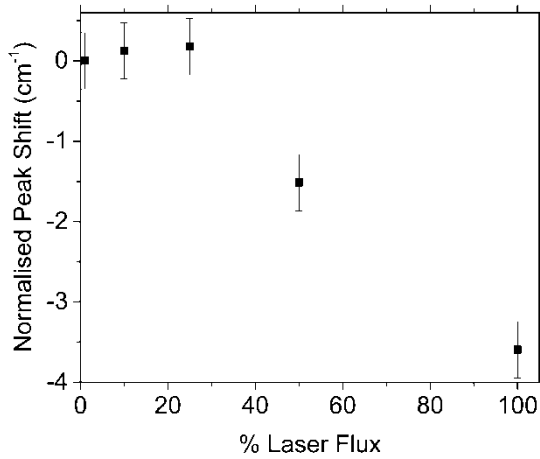


Figure 4.4 Normalised Raman shift as a function of laser flux for 1 μm n-type sample.

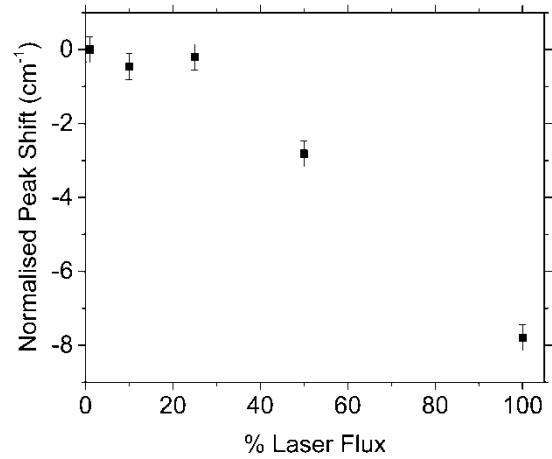


Figure 4.5 Normalised Raman shift as a function of laser flux for 1 μm p-type sample.

4.5.3 Experimental results

Applying this new model to both n- and p-type samples, solutions for thermal conductivity obtained for each sample type are shown in Table 4.1.

Table 4.1 Experimental Results for Thermal Conductivity on both *n*- and *p*-type samples

Sample Type	δ (μm)	Measured Thermal Conductivity (W/mK)			ψ
		This model	2 Omega	Point Source Flux model	
n-type	1	8.5	8.2 +/- 0.4	12.6	0.37
p-type	1	4.2	3.2 +/- 0.3	6.3	0.32

Results obtained demonstrate good correlation with those obtained via a commercial vendor using a complimentary 2 omega technique. The added value of our approach can be found in the fact that samples sent for commercial measurement were destroyed in the process of characterisation.

The improved accuracy offered by our model over existing micro-Raman approaches can also be judged by comparing results with those obtained via the previously used model derived from a point source flux condition as presented in [127]. It can be seen that such an equation provides results for thermal conductivity significantly in excess of those obtained both by this new model and the commercial vendor.

4.6 Discussion

4.6.1 Model accuracy

While the experimental aspects of micro-Raman thermometry and measurement of thermal conductivity are consistent with previous work, the approach presented in this model to derive thermal conductivity from these measurements is new. Typically approaches follow previous work by reference [127] utilising an equation for the calculation of thermal conductivity originally given by reference [145]. Expressed in common terms as per 4.4, where P is absorbed laser power and a laser spot radius this can be given as

$$T = \frac{2P}{\pi(2a)k} \quad (4.27)$$

This equation, originally presented for thermal probe scanning applications uses a prescribed surface flux distribution for a point source located at the centre of a circular contact. With circular contact radius defined as that of the laser spot itself, the use of this flux condition results in values consistently greater than those obtained via equation (4.6) of the model presented in this work.

Consideration of the boundary condition $0 < r \leq a$, $x = 0$ as part of the analysis of the dimensionless thermal restriction parameter ψ suggests that an alternative approach such as that presented here may be needed. While differences in approach may be regarded as having minimal impact when the materials in question possess small values of thermal conductivity, as thermal conductivity increases such variations become increasingly pronounced. This effect is seen in Table 4.1. Indeed, evaluation of results from reference [127] substituting equation (4.6) of our model further demonstrate this. That is, the model presented in this paper obtains a micro-Raman thermal conductivity value for silicon of 43 W/mK at 625°C versus their published value of 63 W/mK. Such a result shows improved correlation with the reported value of 35 W/mK for bulk silicon at 625°C as per their given reference [146].

Sensitivity of any obtained surface temperature to uncertainties in Raman peak position should also be noted. Such uncertainties impact experimentally obtained values for surface temperature and temperature dependent peak shift crucial in establishing laser flux induced temperature change.

While a linear temperature dependent micro-Raman shift of $\sim 0.025 \text{ cm}^{-1} \text{ K}^{-1}$ for silicon between 50°C and 500°C is given in reference [127]; seminal work on Raman scattering from silicon provide theoretical [116] and experimental [147] values suggesting that temperature dependent Raman shift is best represented by a smooth curve rather than a strictly linear relationship, especially when low temperature values are included. A predicted Raman shift value of: i) $0.0185 \text{ cm}^{-1} \text{ K}^{-1}$ for silicon between 100K and 300K and ii) $0.0215 \text{ cm}^{-1} \text{ K}^{-1}$ for silicon between 300K and 500K is given. Experimental measurements between 0K and 770K validate this non-linear prediction. Such values for the silicon transverse Si-Si optical phonon peak shift as a function of temperature are consistent with our own experimental measurements which returned a value of $\sim 0.02 \text{ cm}^{-1} \text{ K}^{-1}$. Caution should therefore be taken when applying fits to experimental data spanning large temperature ranges or when low temperature values are included. Accepting such a value for Raman shift per K, laser induced temperature change is found to be 157°C versus the 125°C originally presented in reference [127]. The recalculation of thermal conductivity via the model as per [127] is now found to yield a value of 52 W/mK. This can again be compared against the value of thermal conductivity obtained using equation (4.6) of the model presented in this work. A value for silicon thermal conductivity of 35 W/mK is returned showing exact agreement with

the expected value. The improved accuracy of this approach remains in line with experimental results demonstrated in section 4.5.

4.6.2 Thermal restriction parameter and determination of substrate effect

Using appropriate mathematical software such as Wolfram Mathematica, solutions for the dimensionless thermal restriction parameter ψ can be readily obtained for any set of input conditions.

Such results can be seen in Figures 4.6 and 4.7 where values of ψ are plotted for given ratios of sample to substrate thermal conductivity, $\frac{k_1}{k_2}$ across a range of $\frac{\delta}{a}$ values.

Figure 4.6 shows calculated thermal restriction parameters for sample thermal conductivities lower than substrate thermal conductivity. Figure 4.7 shows calculated thermal restriction parameters for sample thermal conductivities higher than substrate thermal conductivity. In both figures, values are given for a wide range of possible sample thicknesses.

Keeping the laser radius a fixed, the ratio $\frac{\delta}{a}$ reflects changes in sample thickness. Thus Figure 4.6 and 4.7 present data spanning a variation in sample thickness equal to 4 orders of magnitude. In the case of a laser spot size of $1\mu\text{m}$, this translates as a sample thickness $5\text{ nm} \leq \delta \leq 50\mu\text{m}$.

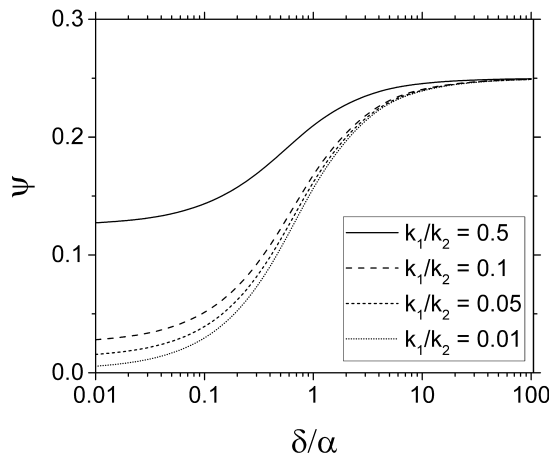


Figure 4.6 Thermal restriction parameter as a function of sample thickness where sample thermal conductivity is lower than that of the substrate.

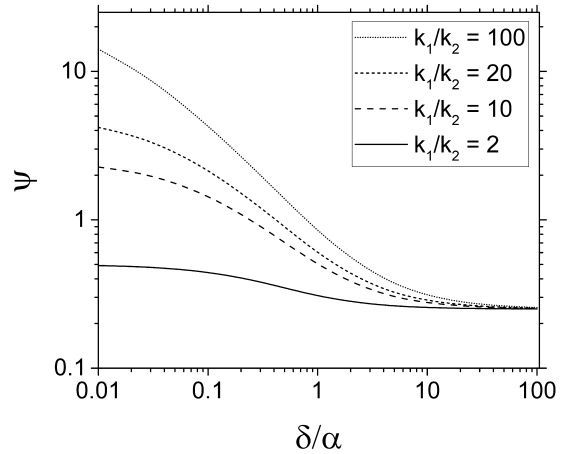


Figure 4.7 Thermal restriction parameter as a function of sample thickness where sample thermal conductivity is higher than that of the substrate.

It can be noted from Figures 4.6 and 4.7 that values of ψ converge towards a value of 0.25. This can be more clearly seen in Figure 4.8. Figure 4.8 presents values of ψ as a

function of $\frac{\delta}{a}$ for three ratios of sample to substrate thermal conductivity: i) Sample thermal conductivity 50% lower than that of the substrate, ii) sample thermal conductivity 50% greater than that of the substrate and iii) sample thermal conductivity equal to that of the substrate. As $\frac{\delta}{a} \rightarrow 100, \psi \rightarrow 0.25$, with the exception of the third condition $k_1 = k_2$. For $k_1 = k_2$, $\psi = 0.25$ for all values of $\frac{\delta}{a}$

We can arrive at an understanding of this effect by evaluating the equation

$$\psi = \frac{k_1}{4k_{apparent}} = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.28)$$

From this it can be seen that $\psi = 0.25$ where $k_1 = k_{apparent}$

This occurs in two situations. Firstly, where $k_1 = k_2$ such that sample and substrate have homogeneous thermal conductivity and thus $k_1 = k_2 = k_{apparent}$

Similarly, where δ is sufficiently large relative to a , substrate thermal conductivity k_2 no longer has any effect on measured values for k and $\psi \rightarrow 0.25$.

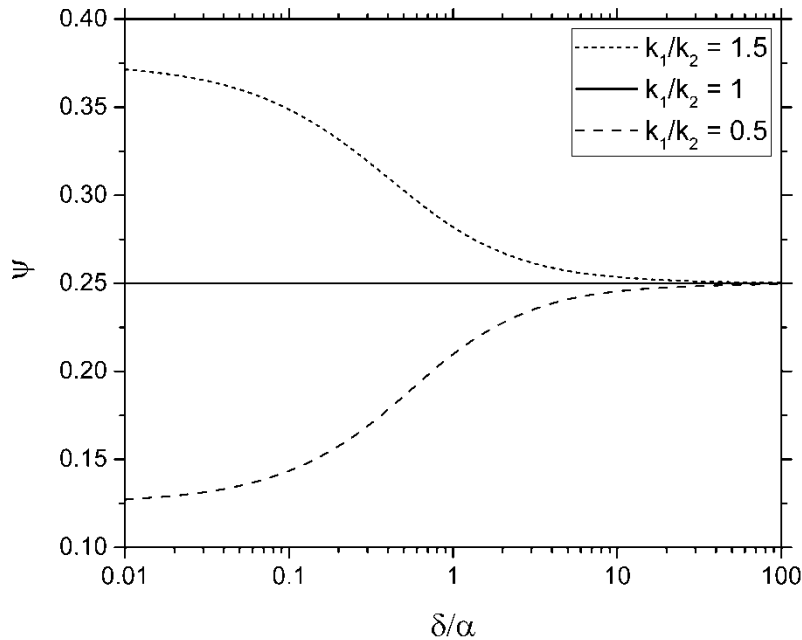


Figure 4.8 Thermal restriction parameter as a function of sample thickness for values of sample thermal conductivity equal to 0.5, 1 and 2 times that of the substrate thermal conductivity.

This relationship allows the effect of any substrate on measured thermal conductivity to be thoroughly evaluated and clarifies whether an experimentally obtained value should be considered apparent or otherwise.

Letting measured thermal conductivity equal k_1 , where

$$\frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \cong 0.25 \quad (4.29)$$

an obtained value of thermal conductivity can be reasonably considered representative of the sample itself.

From Figures 4.6, 4.7 and 4.8 it can be seen that the required thickness for $k_1 = k_{apparent}$ is dependent not only upon the thickness of any sample relative to the laser radius but also upon the relationship of sample and substrate thermal conductivities. Literature commonly suggests that a sample thickness an order of magnitude larger than the laser diameter is sufficient to ensure that substrate thermal conductivity k_2 no longer influences the result [127]. However it can be seen that for many conditions this approximation is insufficient.

4.6.3 Importance of determining sample only thermal conductivities

Assessing values of ψ obtained via measured thermal conductivity values reveals numbers significantly larger than 0.25 for both samples given in Table 4.1. As a consequence, all values shown in Table 4.1 should be taken to represent apparent thermal conductivity rather than expressing a value for the sample itself. With sample thickness only twice that of the laser radius for both samples, the influence of substrate on measured values of thermal conductivity is in line with the expectation that a substrate influence on the measured thermal conductivity of the sample will be present.

Using the model presented in this work, values of sample thermal conductivity can however be estimated. As a result of substrate influence, measured values shown in Table 4.1 represent apparent thermal conductivity. With $k_{apparent}$ known, the equation (4.26) given in section 4.4.2 as

$$\frac{k_1}{4k_{apparent}} = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.30)$$

can be utilised to find the appropriate value for sample thermal conductivity k_1 .

Doing so yields values of 13.8 W/mK and 5.9 W/mK for n-type and p-type samples respectively. Such values demonstrate the importance of obtaining solutions for the

sample alone where substrate influence is present, particularly as values of ψ move increasingly further from a value of 0.25. Where estimations for p-type sample thermal conductivity are 40% greater than the experimentally determined apparent value, estimations for the n-type sample – with a slightly larger value for ψ – can be seen to be over 60% greater than the value of apparent thermal conductivity obtained via measurement.

4.6.4 Suitability of approach

While the approach demonstrated here assumes an isothermal distribution across the laser radius at the surface of the sample under steady state conditions, a high accuracy approach improving upon this condition is presented both in references [142] and [143]. Under this method an isothermal surface condition is required only in the sense of a least squared data fit. Although improvements in results can be achieved with this advanced approach, the arrival at a solution requires markedly increased mathematical complexity. The difference in values of ψ obtained using these high accuracy methods were found to vary by $\leq 6\%$ against the results using the simpler approach utilised in this work.

Assessing the effect of alternative boundary conditions for $0 < r \leq a$ reveals a general insensitivity to selected surface conditions, a view in line with references [139, 142, 143]. The replacement of an isothermal condition with a uniform flux condition for example is found to present a change to the value of ψ where $k_1 = k_{apparent}$ from 0.25 to 0.27. Uncertainty as to the real world boundary condition for $0 < r \leq a$ can thus be considered in terms of this change.

Within the context of micro-Raman based measurement of thermal conductivity, it is our opinion that the approach presented here can be considered appropriate for purpose, especially when weighed against expected uncertainties from the experimental aspects of the micro-Raman thermometry process itself.

4.7 Determination of Thermal Conductivity in this Work

For measurement of samples presented in this work, a comparable micro-Raman spectroscope available at Heriot-Watt University was utilised. This system comprised a Renishaw inVia Raman Microscope fitted with a Leica DMLM microscope stage and a Renishaw nir model 785nm laser. The microscope stage was fitted with a Leica 50x 0.75 objective while the laser offered a maximum power output of 78 mW measured

using a ThorLabs PM100D power meter equipped with a S121C photodiode power sensor. The increased power offered by the laser on this system represents a significant benefit for the measurement of silicon based samples presented within this work. The Si-Si transverse optical phonon peak shift position is an indirect function of laser power. The greater the available power, the greater the peak shift that can be induced providing appropriate levels of sample thermal conductivity are present. For samples where high substrate thermal conductivity results in a relatively high value of apparent thermal conductivity being returned experimentally, the consequence of greater laser power is that a peak position shift can be induced where a weaker laser would be unable to generate a discernable change.

4.7.1 Determination of laser spot size

Knowledge of laser spot size is fundamental for the application of this method and the evaluation of sample thermal conductivity. The experimental determination of thermal conductivity using equation (4.6), and any subsequent evaluation of substrate influence and estimation of sample on thermal conductivity rely on knowledge of this value if a solution is to be obtained.

Measurement of the laser profile revealing beam width at an intensity of $1/e^2$ was undertaken to determine accurately the laser spot size provided by the Renishaw nir 785nm laser and Leica 50x objective.

OFH Optics provide an open source Laser Profile Software that allows the extraction of data points corresponding to laser intensity as a function of width to be obtained in combination with the imaging system present on the Renishaw inVia Raman microscope. This imaging system utilises a Philips ToUcam Pro II camera with a pixel size D_C of $5.6 \mu\text{m} \times 5.6 \mu\text{m}$ allowing the actual dimension per pixel D_A when used with a microscope objective of magnification M to be determined using :

$$D_A = \frac{D_C}{M} \quad (4.31)$$

When used in conjunction with the Leica DMLM stage and 50x objective this translates into an actual dimension per pixel of $0.112 \mu\text{m} \times 0.112 \mu\text{m}$.

Figure 4.9 shows these extracted data points, representing the Gaussian laser beam intensity profile as a function of width. A corresponding Gaussian fit to this data is shown in red. Adjusted R-square value of this fit is found to be 0.997.

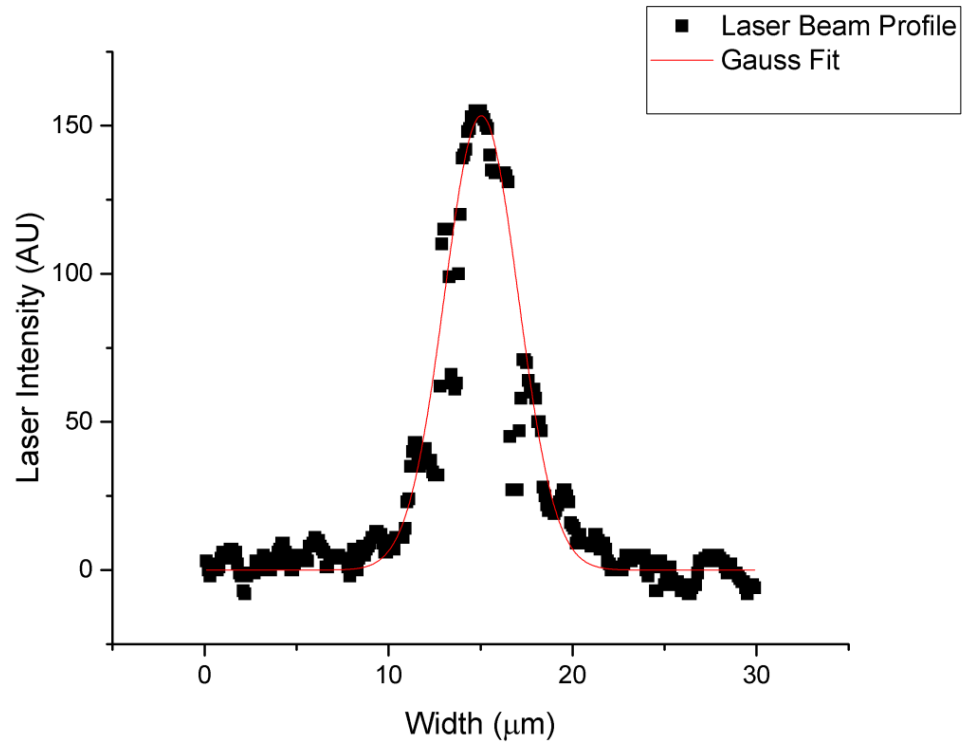


Figure 4.9 Laser Beam Profile showing measurement of beam intensity as a function of width. Data points are extracted from the imaging system on the Raman microscope via OFH open source software. A Gaussian fit to this data is also shown in red.

Using this Gaussian beam profile, an accurate understanding of laser beam spot size at an intensity value of $1/e^2$ is made possible. As shown in Figure 4.10, the horizontal red line representing this $1/e^2$ value is found to intercept the Gaussian laser profile at 11.005 μm and 19.078 μm respectively. Laser beam width is therefore 8.073 μm , showing strong correlation with measurement of laser spot size using a microscope stage ruler.

A composite image showing the laser spot superimposed onto a 100 μm microscope stage ruler featuring 2 μm spacings and 1 μm line thickness shown in Figure 4.11. Here laser spot size is seen to be approximately 8 μm . Note that these values differ significantly from the theoretical ideal spot size obtained using $1.22\lambda/NA$, where λ represents laser wavelength and NA represents the numerical aperture of the objective. For the 785nm laser and 50x 0.75 Leica objective the returned ideal spot size is 1.3 μm revealing the importance of accurate measurement rather than an assumption of ideal size.

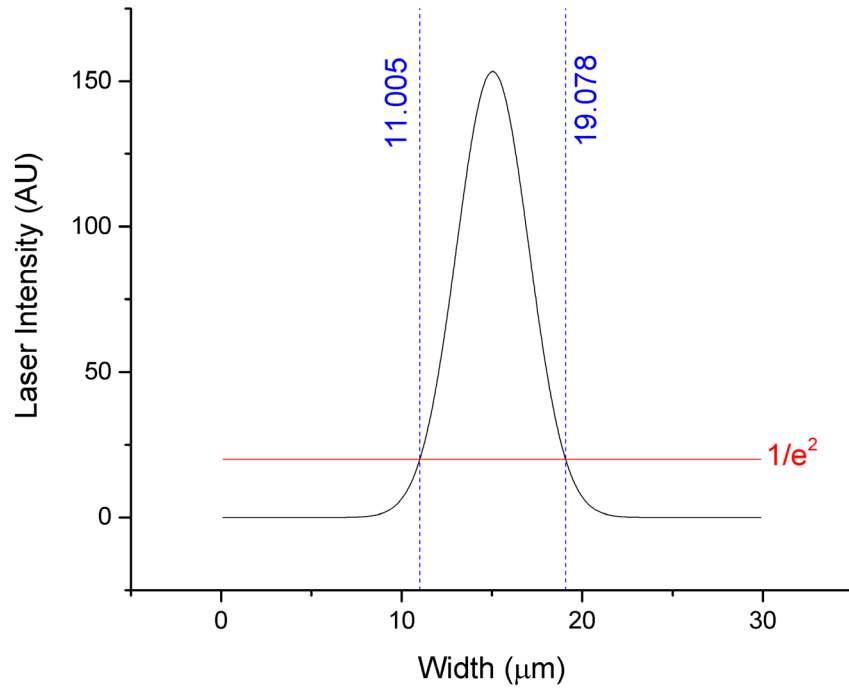


Figure 4.10 Gaussian fit of extracted laser beam profile data and corresponding $1/e^2$ value. The intercepts of this line with the beam profile allows the laser spot size to be calculated. A spot size of $8.075\ \mu\text{m}$ is returned.

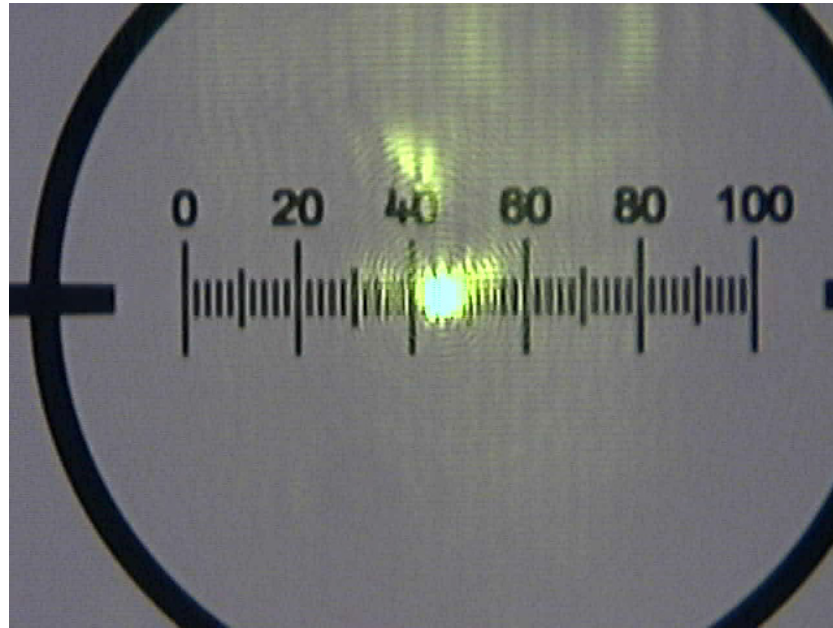


Figure 4.11 Image capture of 785nm laser spot on a $100\ \mu\text{m}$ ruler featuring $2\ \mu\text{m}$ scale lines and $1\ \mu\text{m}$ line thickness.

4.7.2 Methodology

Following calibration of the in-Via Raman Microscope using a reference silicon sample free of defects and impurities in line with manufacturer operating procedures, the

sample under investigation is placed onto a microscope slide on the sample stage and the 50x 0.75 Leica objective positioned above it ready for instrument focussing. For samples with surface texture, focus can be readily obtained visually by the user using the microscope objective and the z axis height adjustment on the Leica DMLM sample stage. In the case of clean silicon samples, a lack of surface features can prevent this approach yielding sufficient accuracy and an alternative approach must be used.

By reducing laser power to values in the range of 10^{-5} %, manual focus of the laser spot itself can be readily undertaken using live video feed from the Philips ToUcam Pro II based imaging system. With laser power safely reduced, the laser aperture is opened via the Wire software interface and adjustment made using z-axis control until optimal focus is achieved. Best focus is signified by a converged laser spot. This approach can be validated by obtaining Raman shift spectra for a range of focus points approaching and beyond converged and comparing peak intensity values. Optimal focus is achieved where peak intensity is maximised.

Raman spectra are then obtained for the sample under investigation using a range of available laser powers, starting at a laser power value where no laser induced temperature effect is produced. For samples investigated during this work, laser powers of 0.5%, 1%, 5%, 10%, 50% and 100% were utilised; and spectra were recorded using 1 second duration acquisitions with 3 accumulations. These parameters were optimised to return an artefact free signal while minimising laser exposure. At high laser powers, acquisition durations greater than 1 second were found to produce artefacts in the collected spectra represented by a clipping at the top of the peak and a loss of data. A discussion of the sensitivity of results to these spectra acquisition and accumulation parameters is included below.

With measurements undertaken for Raman spectra as a function of laser power, spectra data were analysed using PeakFit v4.12. PeakFit is a peak analysis tool produced by Systat Software Inc with a range of features developed specifically for spectroscopy. Application to the collected Raman data allows accurate detection and separation of peaks via de-convolution. Using this software, instrument Gaussian smearing is firstly de-convolved from the recorded spectra before accurate de-convolution of peaks within the Stokes Raman scattering can be undertaken. Peak position as a function of laser flux can be readily identified for all measurements.

Analysis of Raman peak position wavenumbers as a function of laser power is then undertaken to establish magnitude of change. Of importance is the peak shift position between minimum and maximum laser powers – representing no temperature effect and maximum temperature effect respectively. This magnitude of change in peak shift position is then translated into a temperature equivalent value using the equation for silicon as:

$$\Delta T = \frac{\Delta \text{Raman Peak Shift}}{0.02 \text{ cm}^{-1} \text{K}^{-1}} \quad (4.32)$$

Laser Power absorbed by the sample is calculated by subtracting minimum laser power in no heating condition from laser power at corresponding peak shift change and multiplying by (1-reflectivity) for the sample under investigation at the wavelength corresponding to the monochromatic source.

An experimentally returned value of thermal conductivity can now be obtained for the sample using equation (4.6) given previously as:

$$k = \frac{P (1 - e^{-2})}{4aT} \quad (4.33)$$

For samples measured in-situ or with a substrate or supporting layer, an evaluation of this experimentally obtained result as discussed in section 4.6.2 is required to quantify the effect of these structures on this value.

By evaluating:

$$\psi = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.34)$$

a determination of sample substrate effect is made by interrogation of the returned values for ψ . Where a value of $\psi \neq 0.25$ is returned, $k_{\text{apparent}} = k_{\text{measured}}$ but $k_1 \neq k_{\text{measured}}$ and a substrate or supporting structure influence is present. Further analysis must be undertaken to determine a value of thermal conductivity for the sample itself.

In this work, Wolfram Mathematica 9 was used to develop and run a script allowing values of ψ to be returned directly with variables k_1 , k_2 , δ , a . This script is given below in Figure 4.12, where $b = \frac{\delta}{a}$ and $k = \frac{k_1}{k_2}$

For all conditions where $\psi \neq 0.25$, an iterative analysis must be undertaken to determine the actual value of k_1 using the equation previously given in (4.26):

$$\frac{k_1}{4k_{\text{apparent}}} = \frac{1}{4} + \frac{2}{\pi} \sum_{n=1}^{\infty} (-1)^n \alpha^n I \quad (4.35)$$

For both sides of the equation, sample thermal conductivity k_1 represents the only unknown variable allowing a solution for k_1 to be found where convergence is obtained.

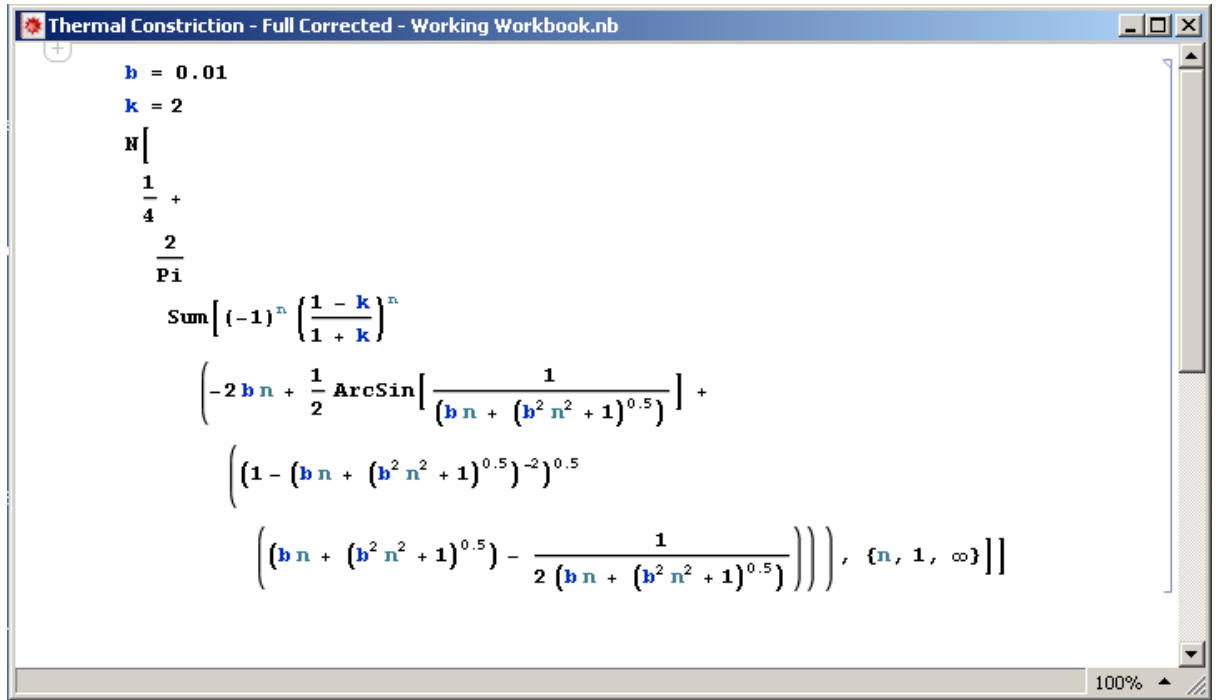


Figure 4.12 Workbook used in Wolfram Mathematica 9 to calculate values for thermal constriction parameter ψ , where b represents the ratio of sample thickness to laser spot size, and k represents the ratio of sample to substrate thermal conductivity.

4.7.3 Sensitivity of results to instrument acquisition and accumulation parameters

During collection of Raman spectra, the operator is free to define experimental parameters for acquisition time and accumulation number. Acquisition time determines the duration of laser exposure – measured in seconds – per measurement, while accumulation number specifies the number of repetitions contained within a single

measurement. These parameters allow optimisation of measurements, ensuring a signal is obtained with appropriate quality. Where acquisition time or accumulation number is too low, a signal with high levels of background noise will be obtained and collected Stokes Raman peaks will be indistinct. Where acquisition times are too long, spectra clipping can occur resulting in a loss of data. In both cases difficulties are encountered achieving accurate peak de-convolution. Additionally, the use of excessive acquisition times and/or accumulations will unnecessarily expose the sample and operator to high levels of irradiation. In order to identify potential experimental sensitivities on obtained Raman peak position to variations in these parameter conditions, a series of measurements were undertaken on 3 sample types.

Samples selected were i) defect free bulk silicon representing a reference, calibration sample, ii) free standing 2 μm silicon film with defects, and iii) silicon-on-insulator featuring an $\sim 2 \mu\text{m}$ device layer thickness containing defects. These samples represented the range of sample types typically investigated during this work.

For each sample, a series of measurements as per Table 4.2 was completed, with each combination of laser power and acquisition time undergoing measurement with 1 and 10 accumulations per measurement. Sensitivity as a function of accumulation number and acquisition time would be established for a full range of possible parameters.

Table 4.2 Measurement conditions for the determination of Raman peak position sensitivity to acquisition time and number of accumulations per measurement.

Sample Type	Laser Power (%)	Acquisition Time (s)	No of Accumulations	
			(a)	(b)
i) Bulk Si ii) Free Standing Si Film iii) SOI	1	1	1	10
	100	1	1	10
	1	3	1	10
	100	3	1	10
	1	5	1	10
	100	5	1	10
	1	10	1	10
	100	10	1	10
	1	10	1	10
	100	10	1	10

Table 4.3 details the mean values obtained for each sample for laser powers of 1% and 100% along with standard deviations of each data set. Peak position was found to be

consistent for each group of measurements and in each case, the small standard deviation returned confirms these findings. No significant influence on obtained values of Raman peak position is found as a result of variation in acquisition time or number of accumulations selected.

Table 4.3 Mean values Raman peak position values obtained as a function of laser powers of i) 1% and ii) 100% for 3 sample types measured using the range of accumulations and acquisitions detailed in Table 4.2

Sample Type	Laser Power (%)	Mean Raman Peak (cm ⁻¹) (μ)	Standard deviation (σ)	$\mu - \sigma$	$\mu + \sigma$
i) Bulk Si	1	521.15	0.016	521.134	521.166
	100	521.14	0.018	521.122	521.158
ii) Free Standing Si Film	1	521.16	0.016	521.144	521.176
	100	511.65	0.105	511.545	511.755
iii) SOI	1	521.19	0.032	521.158	521.222
	100	518.41	0.068	518.342	518.478

In line with expectations, changes in laser power can be seen to influence peak position shift for the samples containing defects and therefore relatively low levels of thermal conductivity. When measured with 100% laser power, Raman peak position was recorded as 511.65 cm⁻¹ and 518.41 cm⁻¹ for the free standing Si film and SOI wafer respectively. This can be compared to the Raman peak position of ~521 cm⁻¹ obtained for the same samples when investigated using 1% laser power and again for all measurements irrespective of laser power on the reference bulk Si sample expected to contain high relative levels of thermal conductivity.

Importantly, where sensitivity to laser power is demonstrated, a corresponding sensitivity to acquisition and accumulation parameter was not found. Raman peak position can therefore be considered insensitive to choice of accumulation number or acquisition length parameter, while remaining sensitive to choice of laser power introduced.

For all samples and parameter combinations, maximum scatter of obtained Raman peak positions relative to calculate mean peak position values were found to be $\leq \pm 0.16$ cm⁻¹, a value well within expectations of instrument resolution. As a result, the optimisation of accumulation and acquisition parameters can be freely undertaken to

obtain best signal quality without an expectation of interference with experimental results. These findings are in line with expectations from theory, where electron response to the incident light source is instant and scattered photon energy a function of a virtual state.

In addition, the low values obtained for both standard deviation and total scatter suggest that by applying appropriate line fitting to Raman spectra, peak positional certainty significantly better than the per pixel resolution of the Raman apparatus itself can be obtained.

Chapter 5: TCAD Simulation and Experimental Design

5.1 Introduction

Careful control of experimental design must be utilised if successful application of the vacancy defect engineering process is to be achieved. A region rich in net concentrations of vacancy defects must be created while damage levels during implantation controlled to prevent complete amorphisation. While an amorphous material is strongly beneficial to a reduced thermal conductivity, for a thermoelectric material the preservation of electrical conductivity is also paramount. Investigations of sample morphology following an introduction of vacancy type defect supersaturations are limited by factors of cost and practicality, while experimental costs related to high energy ion implantation can become large if numerous repeats are required. As a result, simply iterating to an optimal set of experimental parameters via a cycle of manufacture/characterise/evaluate is an inefficient means to obtain insight into suitable sample manufacturing parameters.

Simulation instead must be undertaken in order to identify suitable implant conditions and accurately inform experimental design. Silvaco TCAD, an electronic design automation software platform designed to allow modelling of semiconductor fabrication and device operation provides an industry standard solution. The Athena process simulation package component of this platform offers a computer based solution capable of providing 2D numerical, physically based simulation of semiconductor processing. When undertaken in conjunction with SSuprem4 tools, the simulation of ion implantation and associated damage allows development and optimisation of the defect engineering process to be undertaken without significant expense in wafers and beam time. The implantation simulation within Athena offers both experimentally verified analytical models and Binary Collision Approximation (BCA) Monte Carlo calculations for crystalline and amorphous materials. Flexible control of implant process parameters are combined with universal tilt and rotation control allowing experimental parameters and substrate orientation to be optimised and effects included in simulation outcomes.

Using Silvaco Athena, a range of experimental simulations are possible – varying implant energies, process parameters and substrate structures – allowing the investigation of both magnitude and spatial distribution of point-defects created by the self-implantation of silicon and SOI substrates. From these simulation results,

distributions of damage concentration as a function of depth can be extracted using a modified version of the Net Recoil Density algorithm [148] where net defect distribution ($C(x)$) is calculated as $C(x) = Si(x) + I(x) - V(x)$ where $Si(x)$, $I(x)$ and $V(x)$ represent distributions of implanted silicon ions, interstitial silicon defects and vacancy defects respectively.

5.2 Effects of Implant Parameters Relating to Energy and Fluence

The implant simulation model offered by Silvaco TCAD offers flexibility to control numerous process related parameters. For a correctly defined model and substrate design, parameters relating to implant energy and fluence represent the most significant of these user controllable variables. A series of simulations were undertaken as a means of determining the effect each of each variable on the vacancy rich regions created within silicon substrate targets. Understanding the changes in implant damage produced by these user controlled variables is important if optimised experimental design is to be achieved for a given substrate. Each will be discussed here and effects on the vacancy rich regions produced by this defect engineering process shown. Following simulation, net defect distributions are calculated using the modified Net Recoil Density algorithm provided in section 5.1.

5.2.1 Implant energy

Using Silvaco TCAD, implant simulations targeting a 1 μm thick silicon substrate are undertaken using 3 implant energies ranging from 250 keV to 1000 keV. In each simulation, self-implantation of the target substrate is undertaken at room temperature using a fixed fluence of 5×10^{14} ions/cm².

Results showing net defect distributions of produced vacancies and silicon interstitials for each implant simulation can be seen in Figure 5.1. Concentrations resulting in negative values represent a net concentration of vacancy defects, with a positive value representing a net concentration of silicon interstitials. As implant energy is increased, it can be seen that the depth of any region containing a concentration of net vacancy defects is extended deeper into the substrate. For the lowest implant energy of 250 keV, a vacancy defect rich region can be seen to extend to a depth of only $\sim 0.3 \mu\text{m}$. Beyond this depth net concentrations of silicon interstitials are found. Corresponding depths of net vacancy defect concentrations produced by a 500 keV implant are found to be $\sim 0.65 \mu\text{m}$. As with the 250 keV implant, substrate depths beyond this threshold are found to

be rich in silicon interstitials. Of the three implant energies simulated, only the 1000 keV implant energy is shown to be sufficient to manufacture a sample entirely rich in net vacancy defects. Net vacancy defect concentrations are shown to extend across the full $1\ \mu\text{m}$ sample thickness.

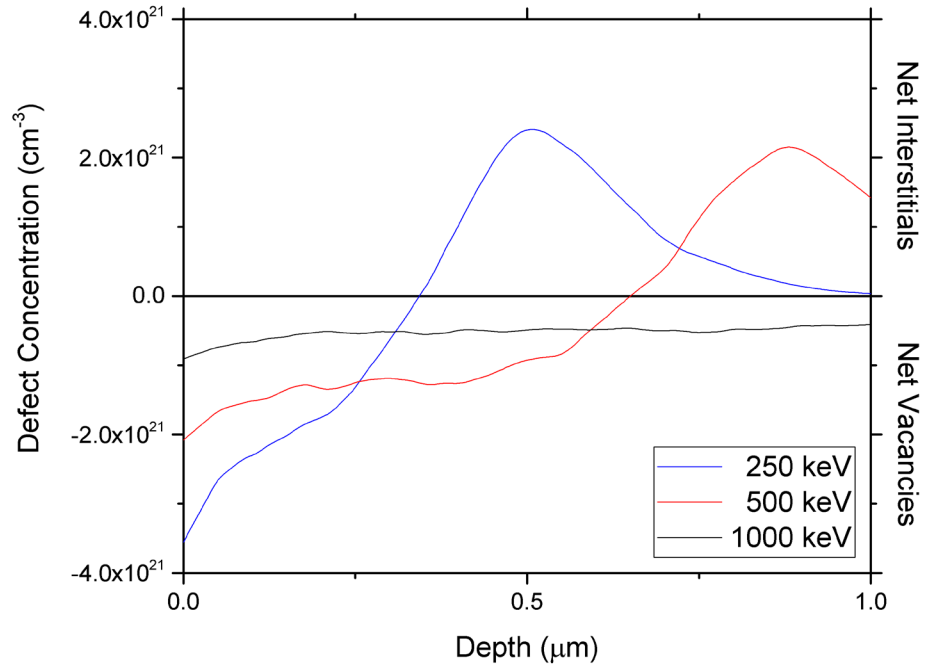


Figure 5.1 Net defect concentrations as a function of target substrate depth for 3 different ion implantation energies ranging from 250 keV to 1 MeV for an implant fluence of $5 \times 10^{14}\ \text{cm}^{-2}$ obtained using Silvaco TCAD simulation. The region containing a net concentration of vacancy type defects is shown by a negative defect concentration while net concentration of silicon interstitials is shown with a positive defect concentration. In the case of an implant with a 1 MeV energy, a region of net vacancy type defects is found to extend across the entire sample thickness.

5.2.2 Implant fluence

Using a $1\ \mu\text{m}$ thick bulk silicon target substrate defined similarly as that simulated for investigations into effects of implant energy, implant simulations are undertaken using a fixed energy of 1000 keV at room temperature. Fluence is varied between $1 \times 10^{14}\ \text{cm}^{-2}$ and $5 \times 10^{15}\ \text{cm}^{-2}$.

Results of these simulations can be seen in Figure 5.2. With each simulated implant capable of producing a net concentration of vacancy defects across the entire sample thickness, Figure 5.2 identifies changes in net vacancy defect concentrations as a function of sample thickness for each ion fluence simulated. In line with expectations, the greater the implant fluence the greater the concentration of net vacancy defects produced. Control of implant fluence offers a practical means of varying defect

concentration. Sufficient concentrations can be sought while avoiding complete sample amorphisation. It should be noted that the vacancy defect concentrations presented in Figure 5.2 represent numbers of individual vacancy defects themselves. At room temperature, mono vacancies are known to be unstable, leading to the formation of stable di-vacancy pairings [149]. The number of V_2 clusters at a given depth will be equal to half that of the concentration of mono vacancy defects shown.

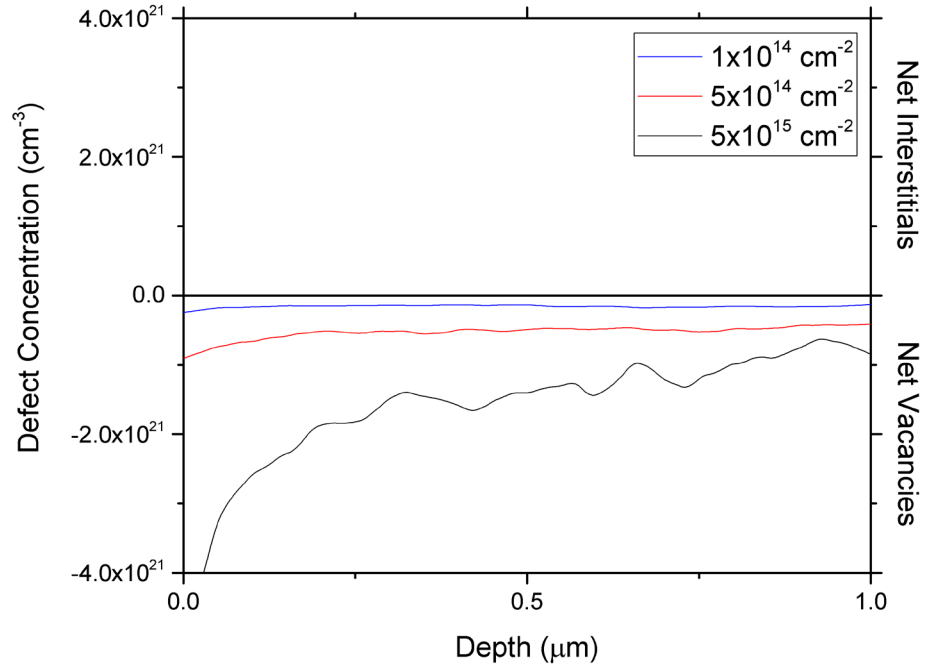


Figure 5.2 Net vacancy defect concentration as a function of sample thickness for 3 high energy ion implantation simulations into a 1 μm thick bulk silicon substrate with varying ion fluences. For all implant conditions a region of net vacancy defects shown as a negative defect concentration is seen to extend across the full thickness of the sample. The higher fluence is found to produce a greater concentration of net vacancy defects.

5.3 Experimental Design

By combining the high levels of controlled offered by high energy ion implantation – specifically via implant fluence and energy parameters - with the defect engineering methodologies detailed previously, two sets of experiments can be designed allowing the investigation of;

- i) The up-scaling of the defect engineering technique from a previously reported 100nm to substrates with thicknesses $\geq 1 \mu\text{m}$ suitable for thin-film thermoelectric devices; using both n- and p-type material.
- ii) The development of this technique for bulk materials, testing the removal of requirements for a buried oxide interface.

Both sets of experiments represent significant advancements in knowledge. The first experiment presents an important extension of a previously reported and highly novel technique; allowing an investigation of suitability for up-scaling to materials with thicknesses suitable for real-world application to be combined with an understanding of effects using both n- and p-type material. The second experiment applies such a technique to bulk materials. This has yet to be attempted or reported. Results are expected to provide experimental confirmation of methodology for bulk Si and a determination of suitability for device focused bulk materials.

5.3.1 Experimental Design I – Up-scaling to sample thicknesses $>1\ \mu\text{m}$ with both n- and p-type material

The vacancy defect engineering concept on a 100 nm thick silicon device layer with n-type doping has been previously reported [14] and the potential for up-scaling highlighted. The 100 nm thickness investigated was at least an order of magnitude lower than thicknesses in the range considered suitable for thermoelectric devices using thin-film materials.

In order to design a set of experiments allowing the demonstration of this approach to sample thicknesses $> 1\ \mu\text{m}$, it is first necessary to determine the maximum depth of vacancy defect rich region that can be achieved using the available ion beam at University of Surrey. Previous simulations confirmed that depth of any vacancy defect region is a function of implant energy, and that an implant of 1000 keV can be expected to produce net vacancy concentrations extending across an entire $1\ \mu\text{m}$ thick sample. With a maximum 2 MeV (2000 keV) implant energy available at University of Surrey the range of sample thicknesses capable of being experimentally produced is expected to be substantially $> 1\ \mu\text{m}$.

The results of TCAD simulation using an implant energy of 2 MeV confirm these expectations. Net vacancies are predicted to extend to a depth of $\sim 1.75\ \mu\text{m}$. Such a depth shows strong correlation with experimental results reported by Venzia et al [97] on a silicon substrate targeted by a comparable 2 MeV implant. Vacancy concentrations were also found to extend to $1.75\ \mu\text{m}$. TCAD simulation results are given in Figure 5.3 where concentrations of vacancy defects, silicon interstitials and implanted silicon ions are shown as a function of target substrate depth.

Implanted silicon ions are shown to penetrate the target single crystal silicon substrate to depths of more than $2\text{ }\mu\text{m}$; and a vacancy rich region extending to a depth of $\sim 1.75\text{ }\mu\text{m}$ can also be seen. A region of vacancy type defects can be assumed to be present where vacancy concentrations are greater than corresponding concentrations of silicon interstitials and vice-versa. The intersection of these two concentrations representing the cross over point from a net vacancy concentration to one of net silicon interstitials.

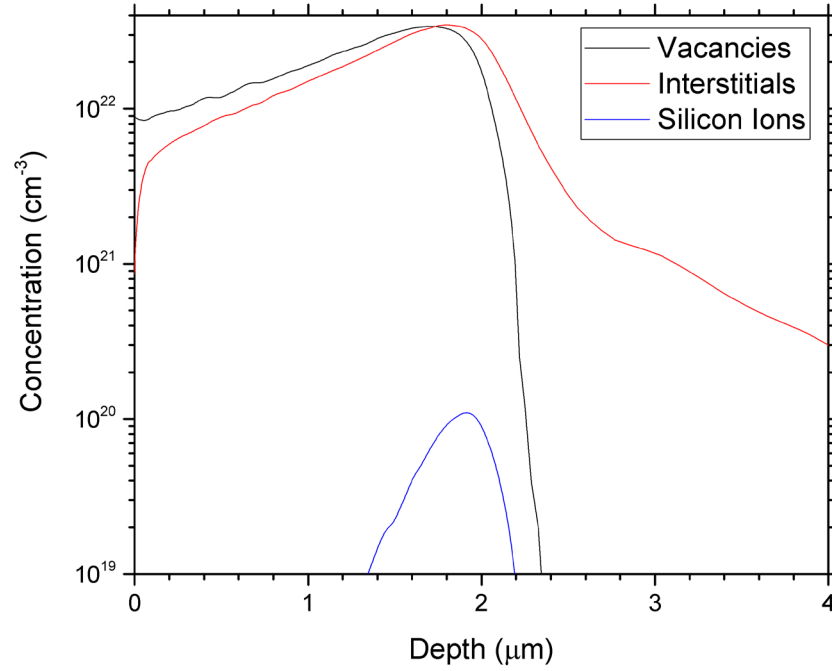


Figure 5.3 TCAD Simulation results showing concentrations of vacancy defects (black), silicon interstitials (red) and implanted silicon ions (blue) as a function of target substrate depth for a high energy ion implantation into a c-Si substrate using an implant energy of 2 MeV. A region of net vacancy defects is found to extend to a depth of $\sim 1.75\text{ }\mu\text{m}$, with a net of silicon interstitials found for target substrate depths greater than this value.

A set of experimental conditions can be readily identified by extending implant simulations to commercially manufactured SOI wafers with device layer thicknesses approximately that of predicted limits identified in Figure 5.3.

Following this series of TCAD simulations, it was determined that self-implantation using an energy of 2 MeV combined with a fluence of $8 \times 10^{15}\text{ ions/cm}^2$ represented an optimal set of conditions for experimental objectives at these device layer thicknesses. Maximised concentrations of vacancy and silicon interstitial pairs could be produced without risk of sample amorphisation. Maximum concentrations of vacancies produced during such an implantation are predicted to reach $\sim 3 \times 10^{22}/\text{cm}^3$. With a silicon

amorphous limit of $5 \times 10^{22}/\text{cm}^3$, such a fluence leaves a suitable safety margin to guard against unintentional amorphisation during the implant process.

The results of a TCAD simulation combining these implant parameters with a commercially available SOI wafer are shown in Figure 5.4. As with Figure 5.3, concentrations of vacancies, silicon interstitials and implanted silicon ions are shown as a function of substrate depth.

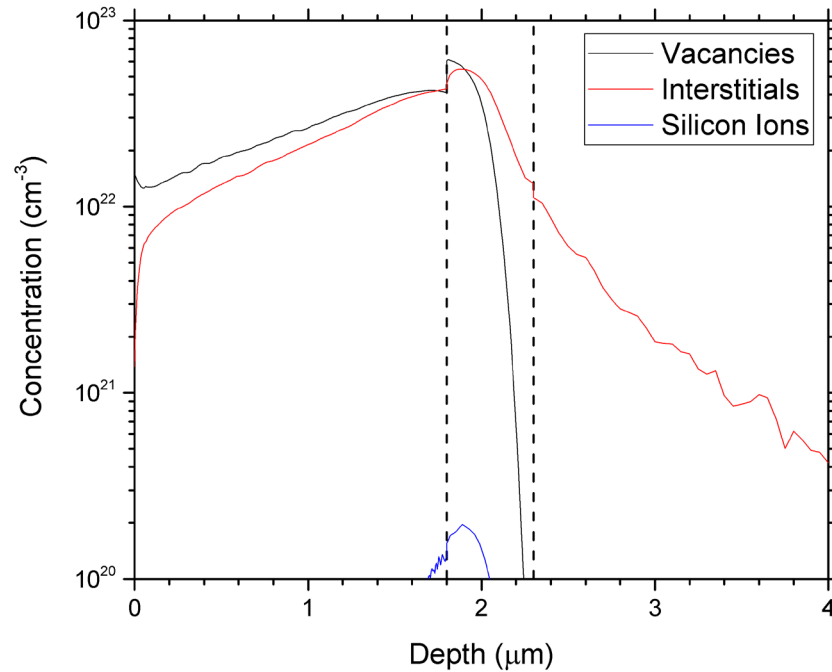


Figure 5.4 TCAD Simulation results showing concentrations of vacancy defects (black), silicon interstitials (red) and implanted silicon ions (blue) as a function of target substrate depth for a high energy ion implantation into a silicon-on-insulator substrate using an implant energy of 2 MeV combined with an implant fluence of 8×10^{15} silicon ions per cm^2 . The SOI substrate is shown with a 1.8 μm device layer above a 0.5 μm layer of buried oxide (identified by vertical dashed lines) and the uppermost region of the thick silicon handling layer.

An SOI structure corresponding to available wafer properties; with the uppermost 1.8 μm device layer followed by 0.5 μm of buried oxide can be seen. Vertical dashed lines delineate the isolating buried oxide layer - 1.8 $\mu\text{m} < \text{depth} < 2.3 \mu\text{m}$. The final layer to the right of the buried oxide, with a depth $\geq 2.3 \mu\text{m}$ represents the first 1.5 μm of underlying silicon handling layer. With such implant conditions, concentrations of vacancies are expected to remain greater than that of silicon interstitials as depth approaches the isolating buried oxide layer while damage concentrations remain below the critical amorphisation level during the implant process.

Using the modified Net Recoil Density Algorithm given in 5.1, concentrations of net vacancy defects and net silicon interstitials can be predicted as a function of target substrate depth from these simulation results, assuming idealised local recombination. Figure 5.5 presents the results of these predictions. With a layer of buried oxide again identifiable by vertical dashed lines, a net concentration of vacancy defects is revealed above the buried oxide layer, and a corresponding net concentration of silicon interstitials present below. The net vacancy concentration following simulated implant and local recombination presents a desirous box like profile, corresponding to an even distribution of vacancies across most of the 1.8 μm thick device layer.

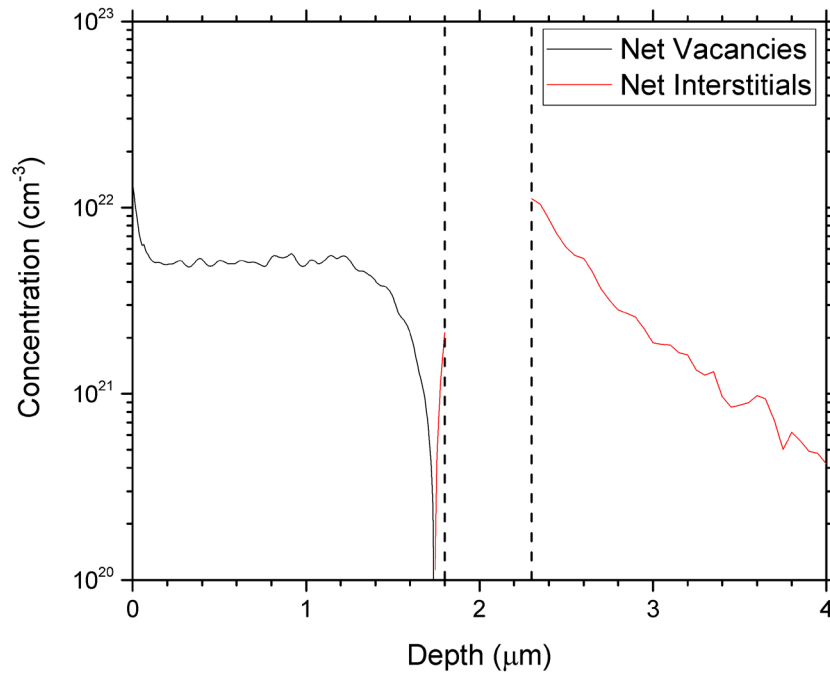


Figure 5.5 Predictions of net vacancy (black) and net silicon interstitial (red) concentrations following a 2 MeV self implantation using a fluence of $8 \times 10^{15} \text{ cm}^{-2}$ with a target SOI substrate featuring a 1.8 μm thick device layer and a 0.5 μm layer of buried oxide. Net concentrations are calculated using a modified version of the Net Recoil Density Algorithm.

It can be noted that the maximum implant energy available of 2 MeV results in a small tail of net interstitials across the final 0.05 μm of this simulated 1.8 μm thick device layer. While either an increase in beam energy, or a reduction in SOI device layer thickness would be capable of removing this entirely, neither was readily available at the time of experimental planning. With concentrations of these residual interstitials small relative to device layer concentration of net vacancies, expectations are that a physical RTA process used for the sample manufacture would see this small concentration of silicon interstitials recombine locally. This can be expected to leave a

purely net vacancy concentration within the 1.8 μm device layer; crucially without significant impact to total vacancy concentration.

Integration of net vacancies present within the device layer following the theoretical recombination of this residual tail reveals an average areal density of vacancies equal to $8.10 \times 10^{17} \text{ cm}^{-2}$. This can be compared to an expected value of $8.16 \times 10^{17} \text{ cm}^{-2}$ were this small interstitial residual not present. Importantly, such a density of vacancies is considerably in excess of the 1.5% vacancy concentration estimated from molecular dynamics studies to achieve a potential 95% reduction in material thermal conductivity [15].

5.3.2 Experimental Design II – Application to free standing materials

Implant conditions identified during Experimental Design I represent a maximum threshold for the safe creation of vacancy defects within a single crystal silicon substrate given the available ion beam at University of Surrey. While Experiment II aims to demonstrate the application of this process to free standing materials, target substrates for experiments using bulk materials remain silicon and are equally limited by this maximum threshold. The challenge for experimental design for Experiment II is one of understanding experimental limitations given the limits of ion beam energy available at University of Surrey and a reliance on off-the-shelf commercially available materials. While an in-house process using an anisotropic wet-etch technique similar to [100] was successful in allowing the manufacture of custom material thickness, achieving sufficient volume of material with appropriate quality control was incompatible with the broader constraints of the project.

A 2 μm thin-film of single crystal silicon manufactured using a wet etch technique before being suspended across a single crystal silicon outer frame of 300 μm thickness for both support and ease of handling was identified via a commercial manufacturer. These samples offer the closest match between available sample thickness and maximum implant conditions possible at University of Surrey's Ion Beam Centre. Nonetheless, this 2 μm sample thickness remains significantly greater than the $\sim 1.75 \mu\text{m}$ maximum depth for net vacancy concentrations simulated to be possible in Figure 5.3. As with Experiment I, a tail of silicon interstitials can be expected to remain within the sample immediately following high energy implantation as a consequence of mismatch between sample thickness and available beam energy. While a post implant RTA can again be anticipated to facilitate local recombination, the increased depth of

this tail – approximately $0.25\ \mu\text{m}$ – requires careful consideration. Too large an interstitial concentration could result in final concentrations of net vacancies insufficient in number to effectively produce a reduction in thermal conductivity.

In order to investigate this effect and ensure appropriate experimental design, TCAD simulation was utilised to study the effects of high energy ion implantation for this combination of sample and implant capabilities. Simulation results utilising an implant energy of 2 MeV, a fluence of $8 \times 10^{15}\ \text{cm}^{-2}$ and a target substrate representing this $2\ \mu\text{m}$ silicon thin film are shown in Figure 5.6.

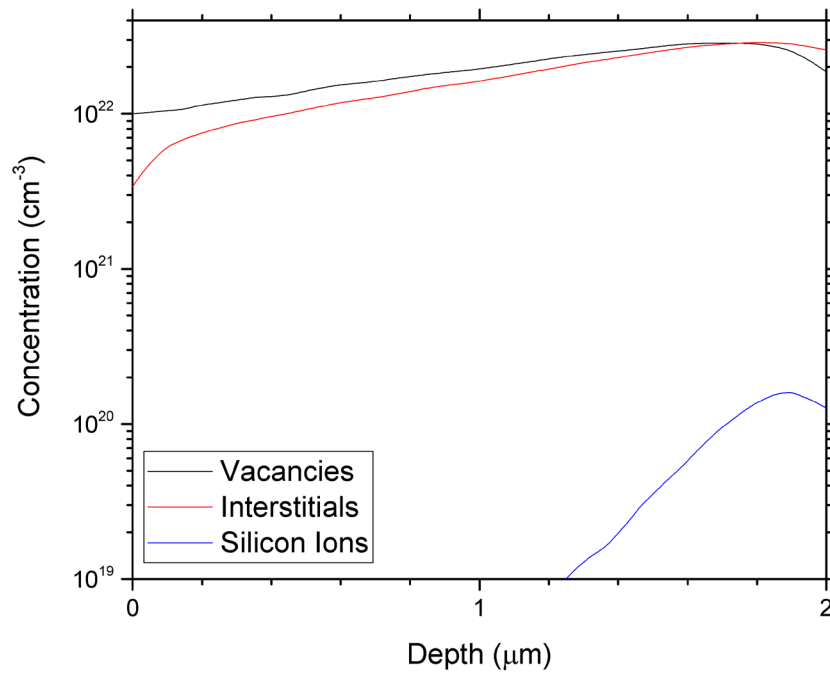


Figure 5.6 TCAD Simulation results showing concentrations of vacancy defects (black), silicon interstitials (red) and implanted silicon ions (blue) as a function of target substrate depth for a high energy ion implantation targeting a $2\ \mu\text{m}$ thin-film c-Si substrate. An implant energy of 2 MeV is combined with an implant fluence of 8×10^{15} silicon ions per cm^2 .

In line with methodology for the creation of a vacancy rich sample using bulk silicon, the implant energy used is seen to penetrate the sample, ejecting a significant amount of both implanted ions and silicon interstitials from the rear of the sample itself.

Using the Net Recoil Density Algorithm as per 5.1 and assuming perfect local recombination allows concentrations of net vacancy defects and silicon interstitials to be calculated as a function of substrate depth. Calculated results using this commercially manufactured $2\ \mu\text{m}$ thin-film silicon substrate are shown in Figure 5.7. Net concentrations of vacancy type defects are predicted to be present to a depth of ~ 1.75

μm . A region featuring a net concentration of silicon interstitials is then seen to extend from $\sim 1.75 \mu\text{m}$ to the edge of the sample at $2 \mu\text{m}$. Such effects are a product of insufficient beam energy. Reducing material thickness or increasing beam energy would be expected to remove this region; leaving a sample featuring only concentrations of net vacancies.

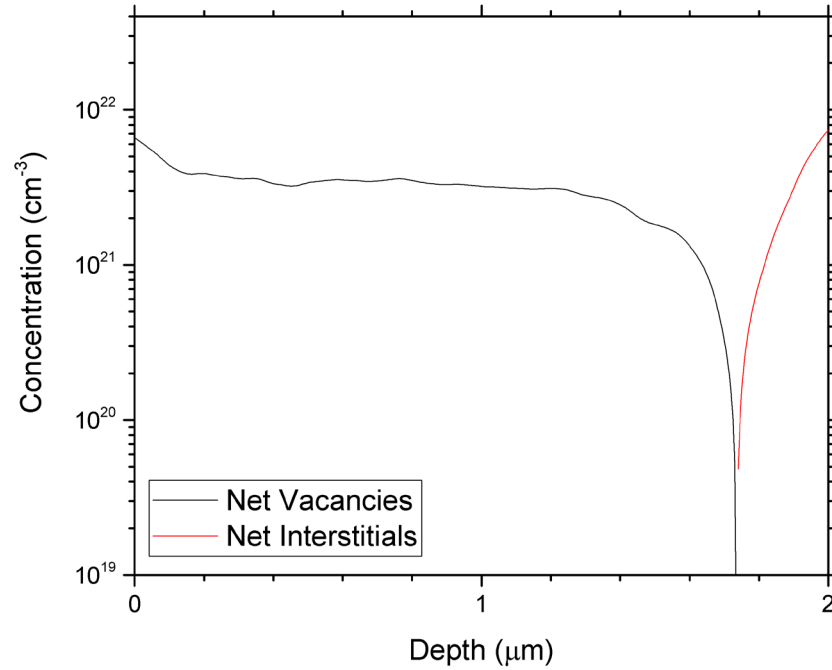


Figure 5.7 Predictions of net vacancy (black) and net silicon interstitial (red) concentrations following a 2 MeV self implantation using a fluence of $8 \times 10^{15} \text{ cm}^{-2}$ with a target substrate of $2 \mu\text{m}$ thick single crystal silicon thin-film material. Net concentrations are calculated using a modified version of the Net Recoil Density Algorithm. A region containing a concentration of net vacancy defects can be seen to extend to a depth of $\sim 1.75 \mu\text{m}$.

The effect of this residual concentration of silicon interstitials on achievable net vacancy concentrations is of significant experimental interest. This interstitial concentration is expected to become mobile during post processing RTA, recombining with local net concentration of vacancy defects and acting to reduce overall vacancy concentrations within the sample. While effects of this residual tail on SOI samples were calculated to be minimal, the increased thickness of this silicon film increases residual interstitial concentration significantly.

Integrating reveals an average areal density of $4.64 \times 10^{17} \text{ cm}^{-2}$ net vacancy defects within the sample following this additional recombination. A density almost half of that produced in the SOI sample with a $1.8 \mu\text{m}$ device layer thickness. While available beam energy is clearly sub optimal for the available sample thickness, the effects on

experimental outcomes are expected to be limited. Not only is a sample rich in net vacancy type defects still predicted following a post implant RTA process but final concentrations of net vacancy defects, despite being lower than possible if experimental parameters were optimised, remain well above the threshold required to test theoretical predictions for effects on reduced thermal conductivity.

5.4 Summary

Silvaco TCAD simulations demonstrate that concentrations of vacancy and silicon interstitial defects resulting from a high energy ion implant are a direct function of implant energy and number of ions implanted; while the average depth of a given ion is a direct function of implant energy used. The adjustment of parameters relating to implant energy and ion fluence allows the region of implanted ions to be controllably located; with control also offered over substrate amorphisation and final net vacancy concentrations. Of importance to this work is the opportunity such control offers for the creation of regions rich in vacancy defect concentrations within targeted silicon samples.

Chapter 6: Experimental Results

6.1 Introduction

Previous chapters highlighted the potential for the vacancy defect engineering approach to be applied to silicon materials with thicknesses suitable for thin-film thermoelectric application. **Experiment I** seeks to apply these identified implant conditions to two commercially available SOI wafers with device layers $\sim 1.8 - 1.9 \mu\text{m}$ thick; experimentally demonstrating process up-scaling and evaluating influence at these increased thicknesses. Samples offer n-type and p-type device layers, allowing evaluation of results for both doping types common in thermoelectric applications. **Experiment II** will apply this defect engineering technique to free standing Si thin-films with a thickness of $2 \mu\text{m}$ allowing demonstration of an approach removing reliance on an isolating layer of buried oxide. Such material offers practical utility in thin-film based thermoelectric devices. In each case, experiments offer significant advancement of applied vacancy engineering as a mechanism for reducing thermal conductivity.

6.2 Sample Selection

6.2.1 SOI samples

As with previously reported work, use of an SOI wafer enables separation of post implant vacancy and silicon interstitial concentrations. Acting as a barrier to cross boundary migration, recombination of vacancy and silicon interstitial outwith individual layers is inhibited during post implant thermal treatments as discussed during Chapter 3. The use of an SOI wafer further facilitates straightforward characterisation of the isolated silicon device layer following processing. All samples used in Experiment I were manufactured from commercially supplied SOI wafer obtained via Ultrasil Corporation, USA featuring a $500 \mu\text{m}$ silicon handling layer beneath a layer of buried oxide and a crystalline silicon device layer. Wafers were selected to allow the full exploitation of available beam conditions at University of Surrey to be balanced against the challenge of obtaining as close a match as possible between samples featuring n-type and p-type dopant species.

Samples used in this study were sourced from sub-sections of each wafer as a means of minimising variation in device layer uniformity and disparity in thickness for n-type and p-type material.

Nonetheless, some manufacturing variation remains between samples obtained from the two selected wafers. Table 6.1 details material properties for each set of samples selected.

Table 6.1 Specifications of samples selected from commercial SOI wafers for use in Experiment I

	Device Layer				Oxide	Handling Layer		
Wafer No.	Type / Dopant	Orientation	Thickness (μm)	Resistivity (ohm.cm)	Thickness (μm)	Type / Dopant	Orientation	Thickness (μm)
1	P/B	<1-0-0>	1.8 ± 0.03	0.005	1	P/B	<1-0-0>	500 ± 10
2	N/Ph	<1-0-0>	1.9 ± 0.12	0.001	2	P/B	<1-0-0>	500 ± 15

Confirmation of electrical characteristics; doping type using Hall effect measurement and conductivity via van der Pauw resistivity measurements were undertaken at room temperature for all samples confirming specifications as per Table 6.1. For all samples, self-implantation combining a beam energy of 2 MeV and a fluence of 8×10^{15} ions/cm² was used. Post implant, the SOI wafers were diced into pieces approximately 12mm x 12mm before undergoing rapid thermal annealing. Samples were annealed using a combination of isochronal and isothermal annealing conditions (3-1000s, 300-1000°C) before undergoing further characterisation, including positron annihilation spectroscopy. Cross plane thermal conductivity for the silicon device layer was obtained at room temperature using a 2-omega system via commercial vendor and a micro-Raman based approach developed and reported during the time of this work.

6.2.2 Free standing Si thin-film

For bulk material, no isolating SiO₂ layer is present to prevent local recombination of vacancy and interstitial. Instead implant energy must be sufficient to directly remove a majority of silicon interstitials from the rear surface of a target substrate. Self-manufacture of bulk samples using an anisotropic wet etch technique as per [100] using a solution of KOH presented initial challenges with quality control that prevented timely use in this experiment. Commercially supplied free standing silicon thin-films were instead investigated. These samples featured a 4.8mm x 4.8mm x 2 μm thick film of (100) c-Si suspended across a 7.5mm x 7.5mm x 300 μm thick c-Si supporting outer frame. These 2 μm films were manufactured using a comparable wet etch technique. Sample thickness is greater than the optimal identified via TCAD simulation given the

available beam energy at University of Surrey; but represents the closest available consumer product at the time of experiments. TCAD simulations presented in Chapter 5 predict that net vacancy defect concentrations should nonetheless be sufficient to achieve targeted reductions in k .

6.3 Vacancy Introduction following Ion Implantation

While the introduction of vacancies via a high energy ion implantation is a feature of semiconductor manufacturing, application of such a technique specifically as a means of reducing thermal conductivity remains novel. Experimental confirmation of both vacancy concentrations and reduced thermal conductivity in a defect engineered sample is yet to be reported. A direct study of vacancy defects is made possible through analysis of as-implanted material using variable energy positron annihilation spectroscopy (VEPAS). The obtained S parameter data as a function of target substrate depth following VEPAS is shown in Figure 6.1, where S parameter is normalised against that of a defect free sample. Such practice appears frequently in literature, allowing for straightforward identification of vacancy rich regions [98, 149-152]. Positrons trapped at sites of vacancy defects return an S parameter greater than that for a defect free sample i.e. $S > 1$ [153].

Ion-implanted silicon is widely held to contain a predominance of stable divacancies (V_2) at room temperature, identifiable by a characteristic S value of ~ 1.04 relative to defect free silicon [149]. Individual vacancies (V_1) are mobile and thus unstable at such temperatures. Data presented in Figure 6.1 reveal a classic VEPAS response to divacancies in SOI, confirming room temperature V_2 concentrations in as-implanted samples in strong agreement with expectations as to both presence and cluster size.

The broad dip revealed in these data as sample depth increases towards $2\text{ }\mu\text{m}$ is explained in part by a natural reduction in vacancy concentrations as substrate depth approaches the $\sim 1.75\text{ }\mu\text{m}$ projected range of initial post implant net vacancies, and in part by the interaction of positrons with the buried oxide layer of the SOI. The S parameter for SiO_2 is reported to be reduced >1 by damage created during ion implantation and acts to influence average S values [98]. The interaction between positron and surface, and positron diffusion length in silicon can be noted to reduce measurement sensitivity in the near surface region. Positrons must be slowed considerably to probe thin films and coatings presenting experimental challenges [153], while diffusion length is typically $\sim 200\text{ nm}$ in crystalline lattices [154]. Comparable

data for the near surface region can be found in [98, 149, 152]. TCAD simulations predict the presence of significant vacancy concentrations in the 0-200nm depth range.

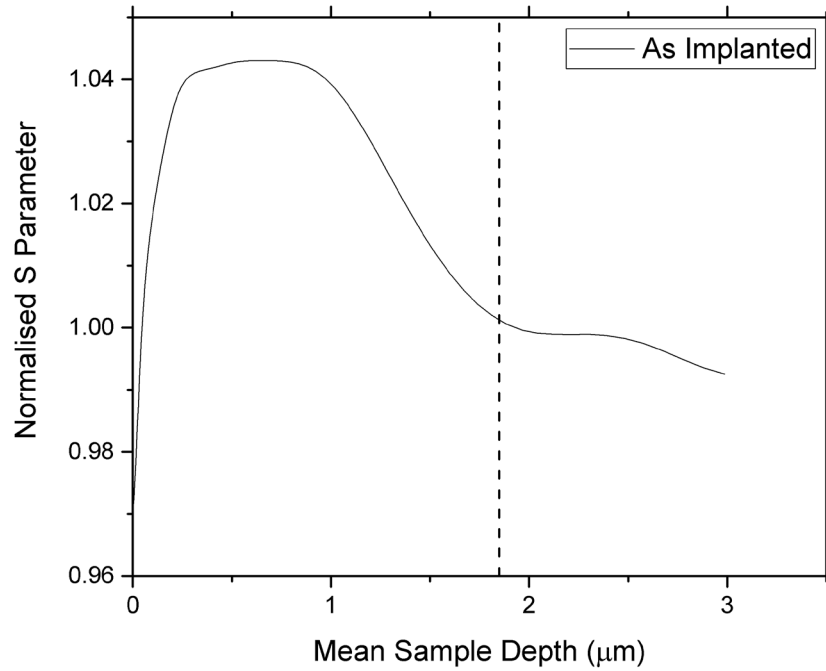


Figure 6.1 Normalised S parameter as a function of target substrate depth following VEPAS analysis on an as-implanted SOI sample. S parameter is normalised against a virgin reference SOI sample. The vertical dashed line approximates the interface between SOI device layer and buried oxide.

6.4 Temperature Dependent Defect Evolution

Literature suggests evolution of vacancy defects can be expected for RTA temperatures $> 350^\circ\text{C}$ in both Si and SOI material [98, 149]. This behaviour has potential implications for targeted reductions in thermal conductivity. NEMD simulations report that reductions in k are sensitive to cluster size for a given vacancy concentration. Larger vacancy clusters are noted to produce less phonon scattering and thus return a higher thermal conductivity than smaller clusters; while cluster size sensitivity is noted to increase as vacancy concentrations reduce [15].

Figure 6.2 presents VEPAS data for samples following isochronal RTA combining 10s duration with temperatures from 600°C to 1000°C . These temperatures align with RTA temperatures identified for electrical and thermal conductivity characterisation studies.

Data is again normalised against that for a defect free sample allowing straightforward identification of vacancy defects. Positrons trapped at vacancy defects reveal a value of $S > 1$ [153].

Following RTA at 600°C, a significant change in vacancy response can be noted. A broadening of the peak and a reduction in average S value are easily identifiable when compared with the strong divacancy response produced by as-implanted material. An explanation is found by considering a reduction in overall vacancy concentration – as defects close to surface or interfacial regions migrate and are lost – combined with an increase in cluster size throughout the sample. Such findings correspond closely with similar studies of defect evolution in ion implanted silicon reported by Coleman et al. Comparable small vacancy clusters remained detectable in vacancy rich c-Si following annealing at this same temperature [98]. Coleman reports the S parameter value for a stable divacancy as ~ 1.04 [149]. The average S parameter for samples following a 600°C anneal shown in Figure 6.2 is below this value, and suggestive of a predominant vacancy cluster size somewhere between V_2 and V_6 . Cluster size is most likely tetravacancies, a dominant size also reported by Coleman in silicon samples annealed at a similar 600°C [149]. For samples annealed at 700°C a change in vacancy behaviour beyond ~ 500 nm is noted. Average S values for depths > 500 nm are found to be slightly lower than for samples annealed at 600°C, suggesting an increase in numbers of hexavacancies at these depths.

A significant change in defect evolution is noted for samples annealed at 900°C. S parameter data reveals an area of persistent vacancy clustering at depths < 500 nm. This is combined with increasingly larger void formation elsewhere in the sample, identifiable by a markedly reduced S value. This is a continuation of a trend noted to begin at 700°C annealing temperatures. Persistent voids in the < 500 nm depth range, where vacancy concentrations are greatest are combined with an increased proportion of larger voids for depths > 500 nm. Average S values returned for samples annealed at 900°C in this study suggest these larger voids may be estimated as ~ 1.8 nm in diameter. A size equivalent to $\sim V_{170}$. Similarly sized voids have been reported for vacancy rich silicon samples annealed at 800°C for a duration of 30 min [98].

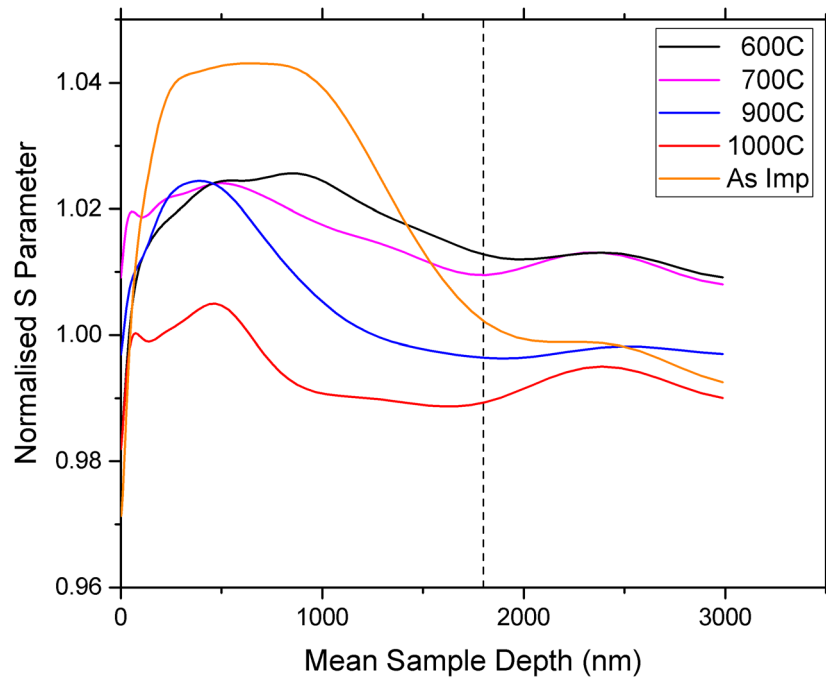


Figure 6.2 Normalised S parameter as a function of target substrate depth and 10s duration isochronal annealing temperature following VEPAS on high energy ion implanted SOI samples. S parameter is normalised against a virgin reference SOI sample not subjected to high energy ion implantation. The vertical dashed line approximates the transition from device layer to the layer of buried oxide.

The identification of regions containing persistent voids is consistent with reported findings of temperature dependent vacancy defect evolution in c-Si [98]. Comparisons of vacancy defect evolution in vacancy engineered and non-vacancy engineered silicon samples undertaken by Coleman et al revealed significantly different behaviours. Implant damage in non-vacancy engineered samples allowed for high levels of vacancy-interstitial annihilation and the return of a sample to pre-implant conditions. In vacancy engineered samples, excess vacancy concentrations instead provide a mechanism for void formation; with voids displaying a resistance to thermally induced recrystallization typical for clusters of concentrated damage. This significant persistence of concentrated damage - in stark contrast to behaviour of scattered damage - was noted by Pelaz et al during molecular dynamics simulations of damage morphology influence on recrystallization in silicon following ion implantation [155]. Recrystallization process dynamics were found to be different for scattered and clustered damage at identical damage concentrations. Where scattered damage was found to allow rapid recrystallization of the silicon lattice during annealing, damage arranged in a concentrated pattern displayed a higher lifetime as a result of increased stability.

For samples annealed at 1000°C, data suggests a small number of now larger voids ($\sim V_{170}$) persist at depths $< 500\text{nm}$. An average S value less than 1 is found for the remainder of the sample. A value of $S=1$ would typically be expected, suggesting - for vacancy engineered samples such as these - the formation of void clusters sufficiently large that positrons are unable to differentiate the internal surface of the void from regular silicon [98]. The average value of $S<1$ following annealing at 1000°C instead suggests migration of oxygen from the buried oxide layer into the device layer. A process known to occur at high temperatures. Implantation damage in SiO_2 can produce oxygen radicals [156]; while the formation of oxygen clusters in Si have been noted to form at temperatures of 800°C [157]. The presence of oxygen is well reported to cause normalised S parameter values lower than that of c-Si [157, 158] and offers a likely explanation for the unexpectedly low S values detected in samples at this temperature.

In summary, the investigation of vacancy defect engineered samples using variable energy positron annihilation spectroscopy confirms the introduction of vacancies and the creation of a vacancy rich device layer. V_2 vacancy clusters are detected in as-implanted samples at room temperature, conforming to expectations about cluster size and stability in this temperature range. For samples subjected to a post implant RTA, temperature dependent defect evolution is shown to occur and cluster sizes estimated. For annealed samples, both concentration and vacancy form are found to be highly dependent on annealing temperature with persistent areas of clusters and voids noted, particularly at depths $< 500\text{nm}$. Effects of this evolution on thermal conductivity can be expected to be significant if theoretical predictions on phonon scattering and cluster size sensitivity are correct.

6.5 Thermal Conductivity in p-type SOI Samples

Room temperature cross plane thermal conductivity as a function of annealing temperature for p-type SOI samples ($1.8\mu\text{m Si}/1\mu\text{m SiO}_2/500\mu\text{m Si}$) containing boron impurities is presented in Figure 6.3. With control samples possessing a room temperature thermal conductivity of 140 W/mK , the effect of the high energy ion implantation on thermal transport is shown to be significant. As-implanted samples return a value of $\sim 3\text{ W/mK}$ displaying considerable reductions. This value approaches the 1.8 W/mK of amorphous silicon [159] and is in close agreement with a previous study presenting proof of principle [14].

Following a 10 second duration RTA at 600°C, room temperature thermal conductivity is found to be ~ 9 W/mK, a modest increase over values obtained for as-implanted samples but still a sizeable 94% reduction relative to control samples. VEPAS analysis reports a reduction in overall vacancy concentrations accompanied by a slight increase in vacancy cluster size in these samples when compared with as-implanted. Both effects are predicted to reduce phonon scattering. For greater annealing temperatures, Figure 6.3 reveals a continuous trend of increasing thermal conductivity. Values of k rise towards that of control samples; slowly until 800°C and then rapidly as temperature increases towards 1000°C.

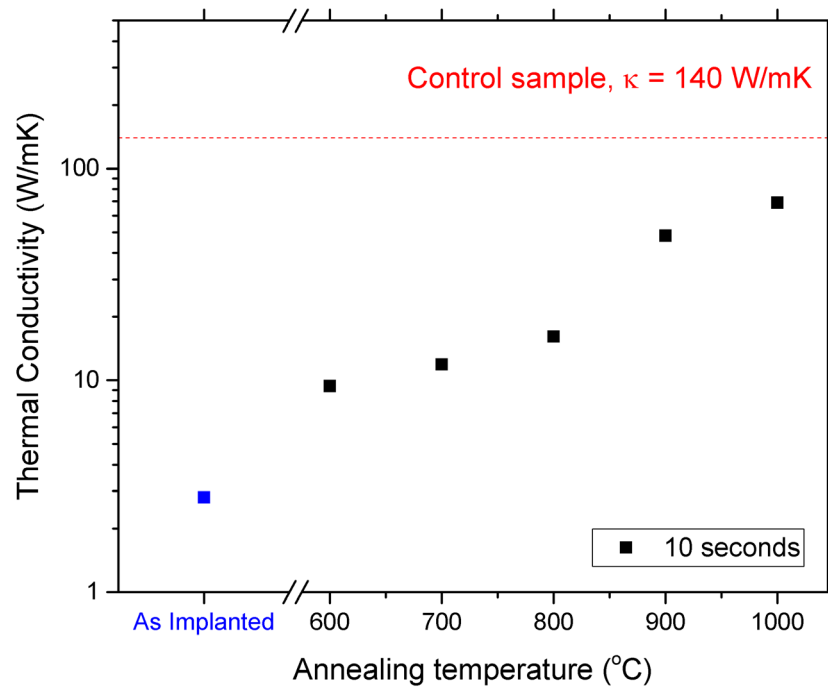


Figure 6.3 Thermal conductivity as a function of RTA temperature for p-type SOI samples ($1.8\mu\text{m}$ Si/ $1\mu\text{m}$ SiO₂/ $500\mu\text{m}$ Si) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{ cm}^{-2}$.

It can be noted that a 1000°C, 10s duration anneal is found to be insufficient to achieve a full restoration of thermal conductivity. Thermal conductivity is measured at 69 W/mK, a value around half that of control samples. Such behaviour is unexpected; especially when considering the significant evolution of vacancy defects measured using VEPAS. Analysis suggests that individual voids are likely sufficiently large as to be indistinguishable by positrons from regular c-Si. Phonon mean free path should be relatively unaffected by such voids given the low numbers expected to be present. A possible explanation may however be found by considering the possibility of oxygen migration identified in Section 6.4. Highly boron doped silicon has been noted to

generate vacancies at temperatures of 700-1000 °C through interaction with oxygen [160]. Here active boron and interstitial oxygen form to create a boron-oxygen complex leaving a lattice site vacancy. Such complexes were also found to produce an S parameter value lower than for crystalline Si – or in the case of a normalised S parameter, a value <1 . It should however be noted that manufacturer literature for the commercial 2ω equipment used for measurement of cross plane thermal conductivity on p-type samples identifies challenges for samples of thickness > 1000 nm as thermal conductivity becomes large [161]. Such limitations are discussed in Chapter 3. While use of this equipment was intended to provide consistency between previously reported results and those produced in this work; such limitations cannot be ignored as a potential explanation for unexpectedly low values of thermal conductivity obtained on p-type samples following RTA at 900 °C and 1000 °C. This limitation is however minimised at low thermal conductivity, leaving good confidence in results presented for ≤ 800 °C annealing temperatures.

VEPAS results presented in Figure 6.2 demonstrate significant numbers of divacancies in these as-implanted samples, with persistent but significantly larger vacancy clusters and voids reported in samples following RTA. Taken together these results experimentally demonstrate large vacancy concentrations and reduced thermal conductivity together in the one sample for the first time; aligning well with theoretical predictions as to their effects in crystalline silicon. Non equilibrium molecular dynamics simulations studied the effects of large vacancy concentrations and associated cluster size on thermal transport in bulk silicon [15]. Thermal conductivity was found to undergo rapid reductions as a result of inhibited phonon transport due to phonon-vacancy interactions. The introduction of vacancies acting to increase phonon scattering and reduce phonon mean free path. At concentrations $< 1.5\%$ the scattering rate displayed a strong cluster size dependence; with small clusters proving more effective at phonon scattering than large clusters for comparable concentrations. For concentrations of vacancy defects $> 1.5\%$, size dependence reduced while a 95% reduction in k over defect free silicon was predicted. Such a prediction is well aligned to experimental results presented here. TCAD simulation predicts a vacancy defect concentration between 8-9% immediately following implantation. Thermal conductivity was reduced by 98%.

It should be noted that the purpose of these high temperature anneals are to allow the study of effects on thermal conductivity and the stability of reductions obtained.

Temperatures greater than 600°C are required to generate significant vacancy evolution. Persistence of V_2 and V_3 vacancy cluster sizes have been previously reported for temperatures of 350°C [98], while evolution to V_4 clusters is reported for 600°C [149] and identified here through VEPAS analysis at the same temperature. V_4 clusters are the smallest size cluster simulated by Lee et al [15]. A size noted to obtain maximum reduction in k during their study. The practical application of this material would not require exposure to operating temperatures at these high levels. Previously reported results have demonstrated long term stability of thermal conductivity reductions achieved by vacancy introduction at temperatures of 150°C [14]. Such a temperature is in excess of expectations as to waste heat from consumer electronics and wearables.

6.6 Thermal Conductivity in n-type SOI Samples

6.6.1 *isochronal annealing between 600°C and 1000°C*

Thermal conductivity measurements for n-type SOI samples ($1.9\ \mu\text{m Si}/2\ \mu\text{m SiO}_2/500\ \mu\text{m Si}$) containing a phosphorus impurity were undertaken at room temperature using a non-contact, non-destructive technique utilising micro-Raman spectroscopy developed during this work and detailed in Chapter 4. Raman shifts for as-implanted samples as a function of system laser power can be seen in Figure 6.4. Raman peak position is presented normalised against Raman peak position measured using a laser power insufficient to induce a localised temperature effect.

This normalisation allows the positional change of Raman peak as a function of increasing laser power to be readily identified. This positional shift corresponds to an equivalent change in local temperature induced by an increasing laser flux, allowing thermal conductivity to be measured through application of this non-contact, non-destructive approach.

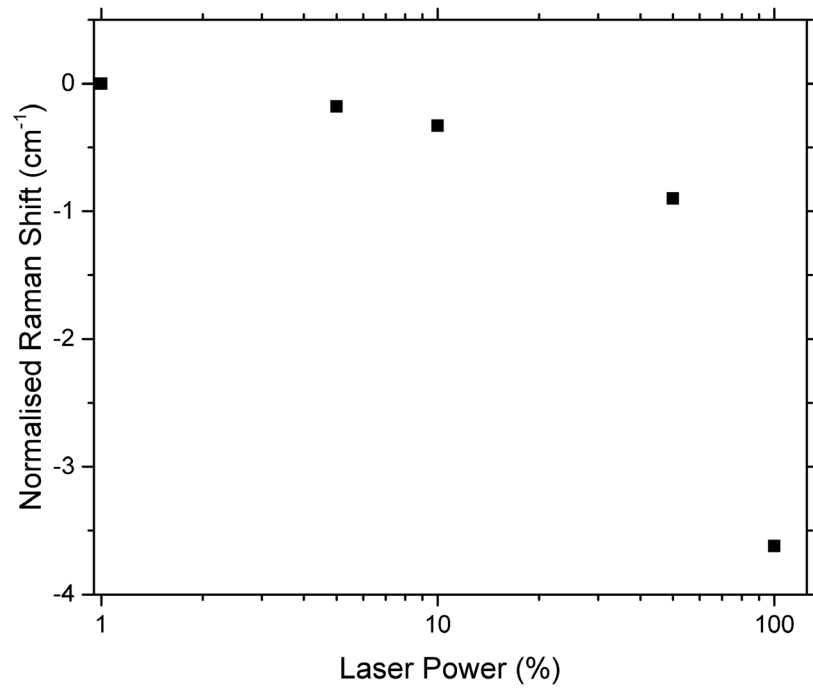


Figure 6.4 Raman shift as a function of laser power relative to Raman peak position using a laser power of 1% for as-implanted n-type SOI samples ($1.9\mu\text{m Si}/2\mu\text{m SiO}_2/500\mu\text{m Si}$)

Figure 6.5 presents measurements of room temperature thermal conductivity for these n-type samples as a function of 10s isochronal annealing at temperatures between 600°C and 1000°C . The effects of high energy ion implantation on obtained estimates of thermal conductivity are significant. Where control samples are found to display a value of $k = 140 \text{ W/mK}$ a thermal conductivity of $\sim 4 \text{ W/mK}$ is found for as-implanted samples. Such a value again approaches the limit for amorphous silicon of 1.8 W/mK as per [159].

Thermal conductivity achieved in these n-type samples is in good agreement with results obtained for p-type samples shown in Figure 6.3 and those reported in literature. Bennett et al found a thermal conductivity of 4.7 W/mK at room temperature in as-implanted SOI with a device layer thickness of 100 nm [14]. Thermal conductivity for as-implanted samples presented in Figure 6.5 is $\sim 97\%$ lower than for control samples, showing strong correlation with theoretical predictions. TCAD simulation again predicts an initial vacancy concentration of between 8 and 9 % immediately after self-implantation.

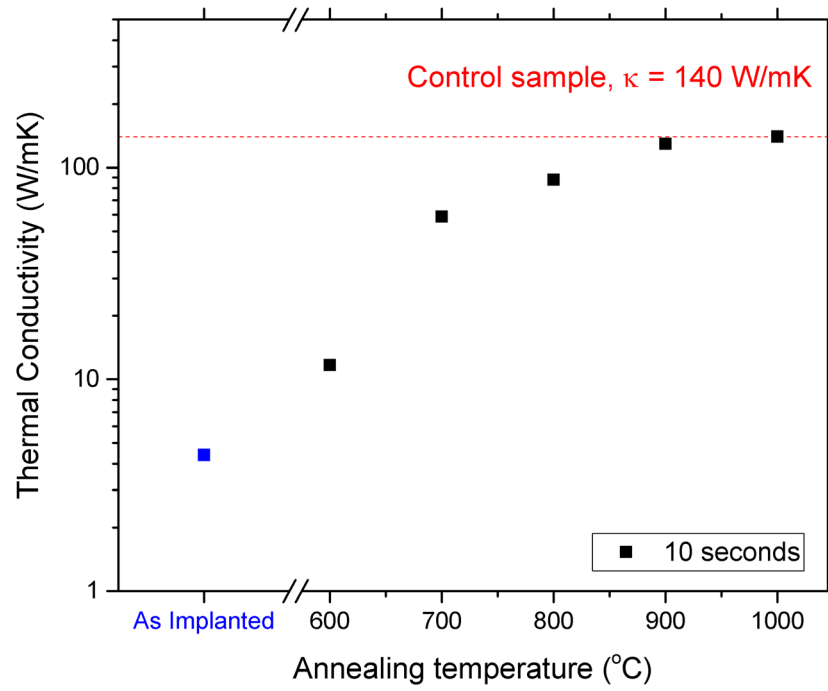


Figure 6.5 Thermal conductivity as a function of RTA temperature for n-type SOI samples ($1.9\mu\text{m Si}/2\mu\text{m SiO}_2/500\mu\text{m Si}$) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{ cm}^{-2}$.

Following a 10s RTA at 600°C, thermal conductivity is measured at ~12 W/mK. Although displaying a modest rise over that of as-implanted samples, this value remains ~91% lower than for un-implanted control samples. These reductions closely follow those found for p-type samples presented in Figure 6.3, suggesting strongly that reductions in thermal conductivity resulting from vacancy defect introduction are achieved independent of impurity type. Such a finding is in line with expectations given impurity concentrations are in the order of 10^{19} cm^{-3} i.e 1 impurity per 1000 Si atoms, however confirmation is nonetheless significant. That reductions in phonon mean free path and increased scattering created through the introduction of large defect concentrations are demonstrated to be equally effective for both dopant types investigated offers value to the broader research community. Particularly since the application of multiscale defects was identified by He & Tritt as a key component of achieving next generation thermoelectric materials [11].

Annealing at temperatures >600°C reveals significant and rapid increases in k , with an annealing temperature of 700°C returning a value of ~59 W/mK and temperatures of 900°C and 1000°C found to restore thermal conductivity to levels in line with control samples. Such behaviour is consistent with the significant temperature dependence of defect evolution presented in Figure 6.2. By 900°C clusters can be expected to have

evolved significantly, with voids approximately V_{170} in size suggested. Such a void is 85 times greater than the predominant divacancy identified in as-implanted samples and significantly larger than the maximum V_{12} cluster size simulated by Lee et al [15]. Effects on phonon scattering can be expected to be limited given low numbers of these larger voids and expectations are that thermal conductivity should be comparable with that of bulk c-Si. Such a view is in line with results presented here. It can be noted that a mechanism reported to produce device layer vacancies in boron doped silicon at high temperatures, where oxygen migration and subsequent boron-oxygen interactions remove boron from lattice site locations is not matched in phosphorus doped silicon [160]. That phosphorus doped samples shown in Figure 6.5 achieve complete restoration while boron doped samples shown in Figure 6.3 do not adds strength to the hypothesis that this mechanism for additional vacancy creation may in part explain the persistently suppressed values of thermal conductivity found for p-type material under high temperature annealing conditions. Reductions in thermal conductivity in as-implanted material are ~95% greater than the best case reductions achievable following exposure at high temperatures. As for p-type material, expected applications do not require such high temperature exposure.

6.6.2 isothermal annealing at 600°C

A second annealing study, featuring isothermal annealing at 600°C was undertaken for durations of 3, 10, 100 and 1000s using n-type samples. Study parameters are in line with previously reported work undertaken on n-type SOI featuring a nanometre scale thick c-Si device layer [14]. Electrical characterisation on self-implanted samples annealed below 500 °C are typified by almost undetectable levels of electrical conductivity, while Pichler suggests that achieving appropriate levels of dopant solubility to allow adequate restoration of electrical conductivity can be challenging below 600°C [162]. Figure 6.5 however reveals significant restoration of thermal conductivity at temperatures $\geq 700^\circ\text{C}$. Annealing for short durations at 600°C offers a best option for identifying changes in thermal conductivity with sufficient resolution to allow identification of best performance.

Figure 6.6 shows cross plane thermal conductivity at room temperature as a function of annealing time for this isothermal study. Measurements were again taken using the micro-Raman based technique detailed in Chapter 4.

An RTA duration of 3s can be seen to produce samples with a thermal conductivity of 6.9 W/mK. A value close to that of as-implanted samples where $k = 4$ W/mK. Reductions remain in strong agreement with expectations as to magnitudes of reductions possible through the introduction of large vacancy concentrations. With a control sample thermal conductivity of 140 W/mK, k following this 3s 600°C RTA remains 95% reduced. A reduction in exact agreement with theoretical predictions.

Thermal conductivity is found to continue to rise as annealing duration is increased. After 10 seconds, $k = 11.7$ W/mK, while a rise in thermal conductivity to $k = 42.2$ W/mK is noted after 100 seconds. Following an annealing duration of 1000s, thermal conductivity is found to have increased considerably to ~ 88 W/mK. Although $\sim 40\%$ lower than that of control samples, such a value is more than an order of magnitude greater than values of thermal conductivity obtained for samples annealed for 3s. While defect cluster size is energy dependent, and thus temperature dependent, the proportion of clusters at this size can be considered a function of annealing duration. Longer RTA durations allow a greater number of the divacancies present in as-implanted material to become mobile and form larger size clusters, reducing phonon scattering effects.

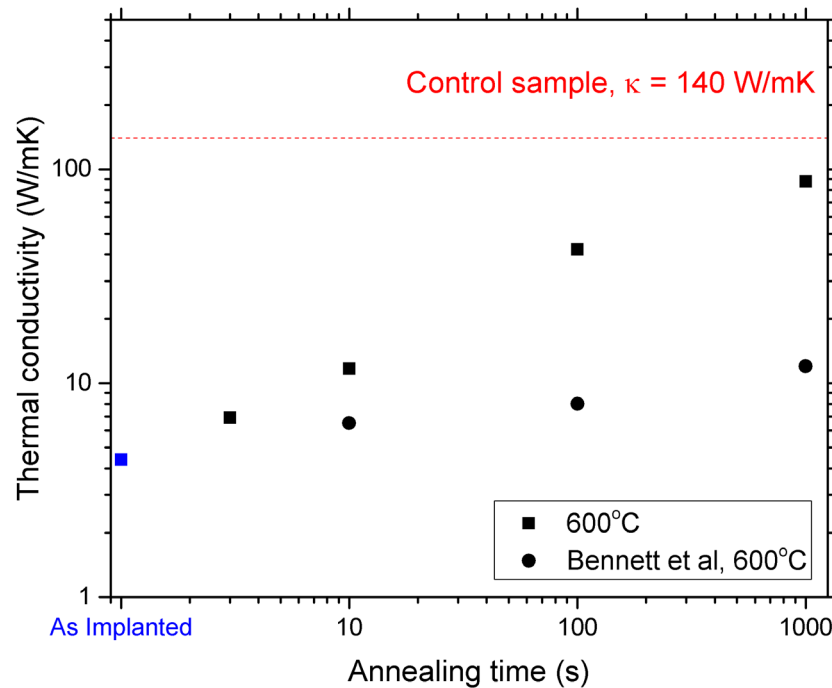


Figure 6.6 Thermal conductivity as a function isothermal annealing at 600°C for n-type SOI samples ($1.9\mu\text{m Si}/2\mu\text{m SiO}_2/500\mu\text{m Si}$) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{ cm}^{-2}$. Also shown are results from Bennett et al - circles - showing reduction in thermal conductivity achieved using vacancy engineering in n-type SOI samples with a significantly smaller 100nm Si device layer [14].

Rates of restoration are found to be considerably faster than was reported by Bennett et al for 100 nm n-type device layers [14]. Values from their study are shown as circles in Figure 6.6. TCAD simulation of the implant undertaken during the manufacture of these 100 nm samples reveals greater vacancy concentrations following self-implantation than for the 1.9 μm thick samples featured in this study. This is in part a result of the increasing influence of high concentration near surface vacancies on overall vacancy concentrations as material thickness reduces, and in part a result of the interstitial tail predicted to remain in these thicker samples at a depth $> 1.75\mu\text{m}$. Predicted range of the initial net vacancy concentration region is $\sim 1.75\mu\text{m}$ as a consequence of maximum available beam energy being limited to 2 MeV at the time of experiments. Vacancy concentrations are one of the two factors theoretically identified to produce increased phonon scattering and reduced values of k , with simulation results identifying an influence on phonon scattering and sensitivity to vacancy cluster size [15]. This larger initial concentration of vacancies may be sufficient to delay the effects of increasing vacancy cluster size on thermal transport reported for 100 nm thick samples by Bennett et al. A disparity in actual annealing temperature as an explanation cannot however be ruled out. A lower temperature for nanometre samples compared to these thin-film samples could potentially explain this disparity. Such an explanation is however unlikely given results of resistivity as a function of RTA duration noted during electrical characterisation and discussed in section 6.9.

6.7 Thermal Conductivity in Free Standing Si thin-film

The application of defect engineering to free standing c-Si thin-films requires a modification of approach over that demonstrated for SOI material. Free standing material has no isolating buried oxide layer to prevent silicon interstitial migration. Instead these silicon interstitials must be ejected from the rear surface of the sample itself if a net vacancy region is to remain following local recombination.

Use of c-Si thin film material free of any supporting layer removes any reliance on oxide layers for success, offering particular utility to thermoelectric applications targeting microharvesting. A c-Si material in free standing form offers a more straightforward approach for device manufacture than a device material fusion bonded to an $\text{SiO}_2/\text{c-Si}$ substrate as in the case of SOI. Application of vacancy defect engineering for the purpose of reducing thermal conductivity has yet to be reported on free-standing material.

Measurements of cross plane thermal conductivity were undertaken at room temperature for free standing silicon thin-films with a thickness of $2\ \mu\text{m}$ using the same micro-Raman technique applied for n-type SOI samples. Figure 6.7 shows the room temperature Raman spectra for an un-implanted control sample as a function of laser power, while Figure 6.8 presents Raman spectra collected from an as-implanted sample following self-implantation at $2\ \text{MeV}$, $8 \times 10^{15}\ \text{ion/cm}^2$. A characteristic Si-Si peak can be clearly identified in all spectra. A vertical dashed line at $521\ \text{cm}^{-1}$ allows the relative positional location of each Si-Si peak to be readily evaluated.

The positional shifts of these Raman peaks under full laser power are easily identified in both Figures. The relative movement of these peaks is shown to be considerably greater for as-implanted material than for implant free control samples. This difference is highly indicative of a lower value of thermal conductivity as per [89, 127]. While factors such as strain are also widely reported to cause shifts in Raman peak position [163], such factors are not considered an explanation here. Significant shifts are shown only to occur under full laser power identifying a flux dependence, while direct effects would be expected to be comparable in both as-implanted and non-implanted material.

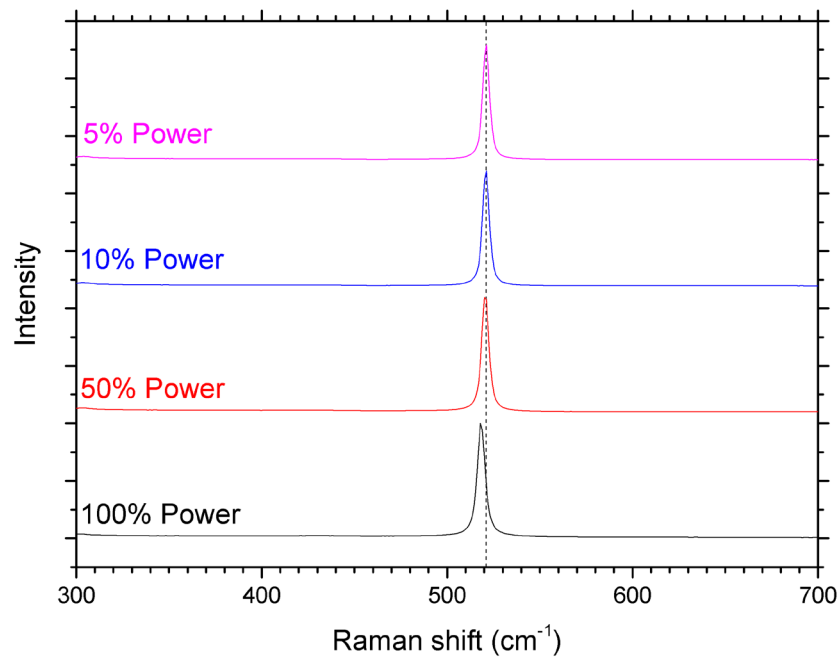


Figure 6.7 Raman spectra as a function of laser power collected from a reference $2\ \mu\text{m}$ free standing Si thin film at room temperature. The characteristic Si-Si peak can be clearly identified for each spectra. A vertical dashed line allows the relative movement of this Si-Si peak position to be easily identified.

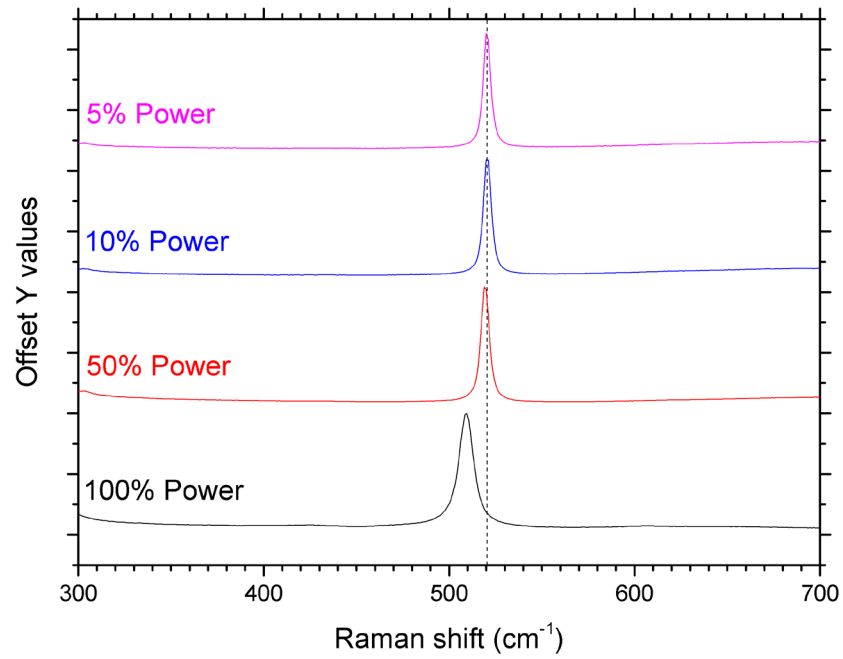


Figure 6.8 Raman spectra as a function of laser power collected from an as-implanted 2 μm free standing Si thin film at room temperature. The characteristic Si-Si peak can be clearly identified in each spectra. A vertical dashed line allows the relative movement of this Si-Si peak position to be easily identified.

The calculation of thermal conductivity using this technique can be readily undertaken using equation (4.6) given in Chapter 4 as:

$$k = \frac{P (1 - e^{-2})}{4aT} \quad (1)$$

Where P represents absorbed laser power, a is laser spot radius and T is equivalent sample temperature obtained using flux dependent shifts in micro Raman peak position.

With samples free standing, returned values of k obtained using equation (1) can be taken as directly representative of the sample itself. No further evaluation to determine substrate influence is required; as would be the case for samples located on substrates or combined in lattices.

Figure 6.9 presents results for cross plane thermal conductivity measured at room temperature for control samples, as-implanted samples and samples subjected to an RTA of 1000s duration at a temperature of 600°C.

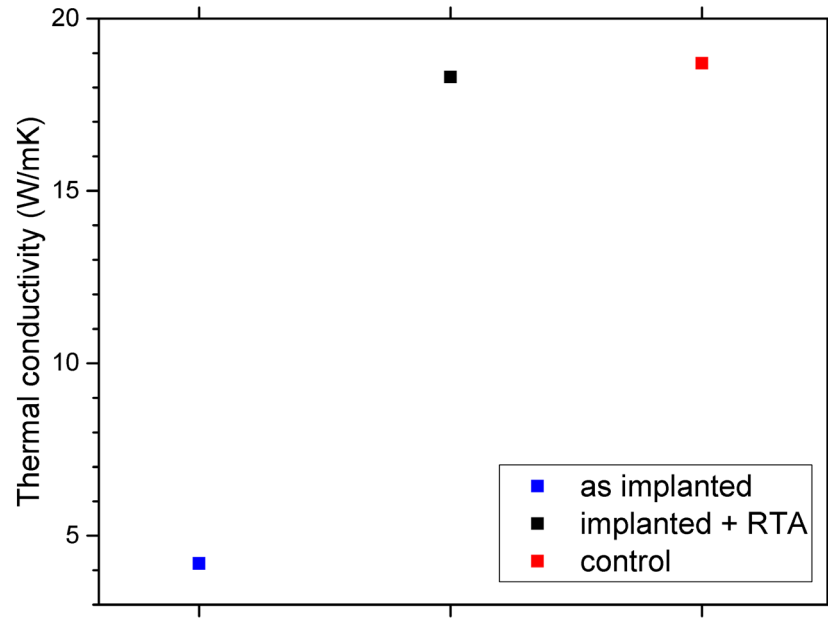


Figure 6.9 Room temperature cross plane thermal conductivity on free standing silicon thin-films of 2 μm thickness. Values for an as-implanted sample and a sample following RTA at 600°C for 1000s can be compared to that of an unimplanted control sample.

As-implanted samples of free standing c-Si thin-film return a value of $k = 4.2 \text{ W/mK}$. Reductions in thermal conductivity show strong correlation with results offered from application of this technique to upscaled SOI material shown in Figures 6.3 and 6.5. Thermal conductivity was found to be $k = 3 \text{ W/mK}$ and $k = 4 \text{ W/mK}$ for as-implanted p-type and n-type SOI respectively. Such results are significant, demonstrating successful application of defect engineering for the purposes of reduced thermal conductivity to free standing material for the first time. The modified defect engineering technique – where no buried oxide layer is present to isolate interstitial migration – is demonstrated to be as effective in reducing thermal conductivity of free standing c-Si material as it is for SOI device layers.

A value of $k = 4.7 \text{ W/mK}$ is reported in literature by Bennett et al for room temperature thermal conductivity in as-implanted silicon nano-films containing a supersaturation of vacancy defects [14]. This value agrees with results for reductions to k found in both bulk and SOI material presented here. An evaluation of these convergent results suggests that a value of $k \approx 4 \text{ W/mK}$ may approximate a lower bound for thermal conductivity in non-amorphised silicon when applying defect engineering. Such an effect is in line with theoretical predictions presented by Lee et al [15]. Vacancy concentrations between 0 and 2 % are simulated and effects on k presented. Thermal conductivity is predicted to experience a reduction of $\sim 95\%$ at 1.5% vacancy

concentration, but undergoes minimal further reduction as concentration is increased $> 1.5\%$. Crucially however, results presented here suggest that reductions achievable using defect engineering may have an absolute limit rather than being strictly proportional.

Following a 1000s RTA at 600°C , thermal conductivity is found to restore to levels comparable with that of un-implanted control samples. This rate of restoration at 600°C exceeds that for SOI samples presented in Figure 6.6. While thermal conductivity measured in free standing, thin-film control samples is considerably lower than for control samples of SOI material shown in Figure 6.6, this relative increase in restoration is still worthy of comment. Initial vacancy concentrations are predicted by TCAD simulation to be approximately half the concentration found in SOI samples featured in this study. A more pronounced end zone of residual silicon interstitials is expected to remain in these thin-film samples as a result of limitations in available beam energy - 2 MeV maximum – and an additional 200nm sample thickness. These factors act to reduce initial net vacancy concentrations. A hypothesis suggesting a link between the rate of thermal conductivity restoration and the magnitude of initial vacancy concentrations was offered as a possible explanation for the difference in restoration rates noted for SOI samples in this study and that reported by Bennett et al [14] at 600°C . Such differences are clearly identifiable from Figure 6.6. The addition of a further disparity in restoration rates noted for free standing thin-films presented in Figure 6.9 and those of SOI in Figure 6.6 when taken in context of initial vacancy concentrations further strengthens this hypothesis.

When viewed broadly, results suggest that vacancy concentrations above a threshold level appear to offer limited returns with respect to further reductions in thermal conductivity. However these increased vacancy concentrations may yet act to slow the rate of restoration for thermal conductivity during RTA. Theory indirectly implies such behaviour. Lee et al predicted a maximum reduction in k at 1.5% vacancy concentration to be matched by a removal of cluster size dependency for vacancy concentrations $> 1.5\%$ [15]. This relationship could offer opportunities to extend RTA duration that would not be obvious if only the relationship between vacancy concentration and absolute reductions of k were considered. Such behaviour may become important for optimisation, but also for manufacturing quality control when RTA durations are measured in seconds.

Free standing control samples were found to have an unexpectedly low thermal conductivity of ~ 19 W/mK. While reduced film thickness is well reported to produce a corresponding reduction in k , effects are generally found only for material thicknesses $< 1 \mu\text{m}$ [68]. A thermal conductivity comparable to bulk would therefore be expected. An explanation for this inherently low value may however be suggested by investigation of sample morphology. An SEM image of this control sample is shown in Figure 6.10 where numerous surface imperfections can be identified with scales in the order of 10^{-9} m.

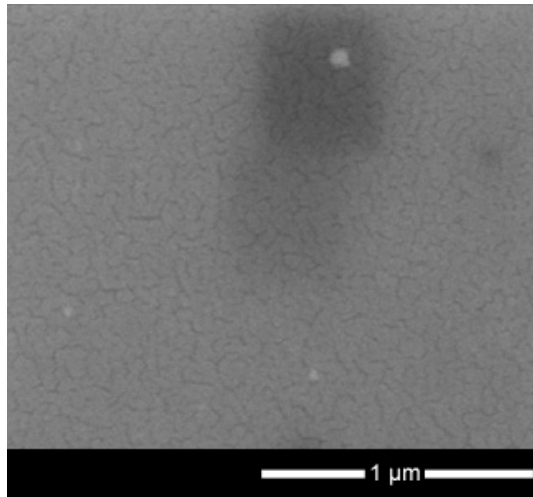


Figure 6.10 SEM image showing the surface of a control sample of $2 \mu\text{m}$ thick silicon thin-film manufactured using a wet etch technique. Numerous imperfections can be noted across the surface.

Similar, but more defined imperfections can be seen reported during wet etching of silicon, where surface cracking, flaking and porosity have been noted as a result of the etching process [164, 165]. Such morphology may offer an explanation for the reduced thermal conductivity found on control samples by offering sites for phonon scattering not typical of c-Si.

6.8 Summary of Effects on Thermal Conductivity

Defect engineering is shown to produce significant reductions in thermal conductivity for both SOI and free standing c-Si thin films. Success reported in 100 nm device layer thickness SOI by Bennett et al [14] is shown to be translatable to significantly greater thicknesses where material has application utility. Adaptation of the process, removing a requirement for samples to contain an isolating layer of buried oxide is demonstrated and results with free-standing material shown to be comparable with those obtained using SOI. Materials up to $2 \mu\text{m}$ are tested and thermal conductivity found to be ~ 4

W/mK, a significant 97% reduction over thermal conductivity of bulk c-Si. In all cases, reductions agree well with theoretical predictions offered by Lee et al where reductions of 95% were suggested via simulation [15]. Importantly, reductions in thermal conductivity are found to be independent of doping type. With multiscale defect engineering identified as a key for development of next generation thermoelectric materials by He and Tritt [11], findings suggesting independence of result from impurity are significant for other research groups considering alternative materials. Results identify two further potential effects that may offer significance. Firstly, a threshold for reductions to k appears to be approximately 4 W/mK, suggesting a relationship between vacancy concentrations and reductions in thermal conductivity that may offer a more absolute limit rather than the proportional limit reported by theory [15]. Secondly, increasing vacancy concentrations beyond that required to achieve maximum reductions in k may act to slow the rate with which thermal conductivity is restored during RTA. A finding with potential benefits for large scale material manufacturing. Reductions in thermal conductivity achieved using defect engineering can be compared to alternative approaches for silicon thermoelectric material. Hochbaum et al reported a value of $k = 1.6$ W/mK for 52 nm thick nanowires featuring surface roughness [8]. 115 nm thick nanowires were found to return a value of $k = 8$ W/mK. 100 nm thick nanoporous silicon membranes were reported by Tang et al to display a thermal conductivity of ~ 2 W/mK as a result of significant phonon disruption [69]. Reductions reported in this study are in line with those found in these materials. Importantly however, the reductions in thermal conductivity achieved through defect engineering leave materials that are visually indistinguishable from bulk c-Si and which are free from dimensional nanodependence; potentially transformational for Si-based thermoelectrics.

6.9 Electrical Resistivity

6.9.1 *p-type SOI samples*

Figure 6.11 shows electrical resistivity for p-type SOI samples as a function of annealing time and temperature. In line with expectations, samples immediately following ion-implantation are found to possess undetectable levels of electrical transport as a result of typical implant induced damage and are not shown. High energy implants are well known to produce dopant displacement and lattice disorder (associated charge carrier scattering). Both act to increase electrical resistivity.

Similarly undetectable levels of electrical conductivity are found for samples following RTA at temperatures $< 500^{\circ}\text{C}$.

For samples subjected to RTA temperatures $\geq 500^{\circ}\text{C}$, a strong temperature dependence to improvements in electrical conductivity are noted, in line with expectations regarding recrystallization and an emerging reactivation of phosphorus dopant. For an RTA duration of 1000s at 900°C , and both RTA durations undertaken at a temperature of 1000°C , resistivity was found to have restored to almost that of un-implanted control samples. For temperatures $\leq 900^{\circ}\text{C}$ restoration for 1000s duration is found to be greater than for 10s duration.

These temperatures required for a full restoration of electrical conductivity are in line with literature. For p-type samples featured in this work, impurity concentrations are in the order of 10^{19} cm^{-3} . Plots of solubility as a function of temperature suggest annealing temperatures $> 800^{\circ}\text{C}$ are required to achieve comparable concentrations [162]. Characterisation of silicon containing boron impurities following ion implantation reported a requirement for an annealing temperature $\geq 900^{\circ}\text{C}$ to achieve such concentrations [166]. Additionally, significant reductions in electrical conductivity for RTA temperatures below 900°C are found; a finding in agreement with Figure 6.11.

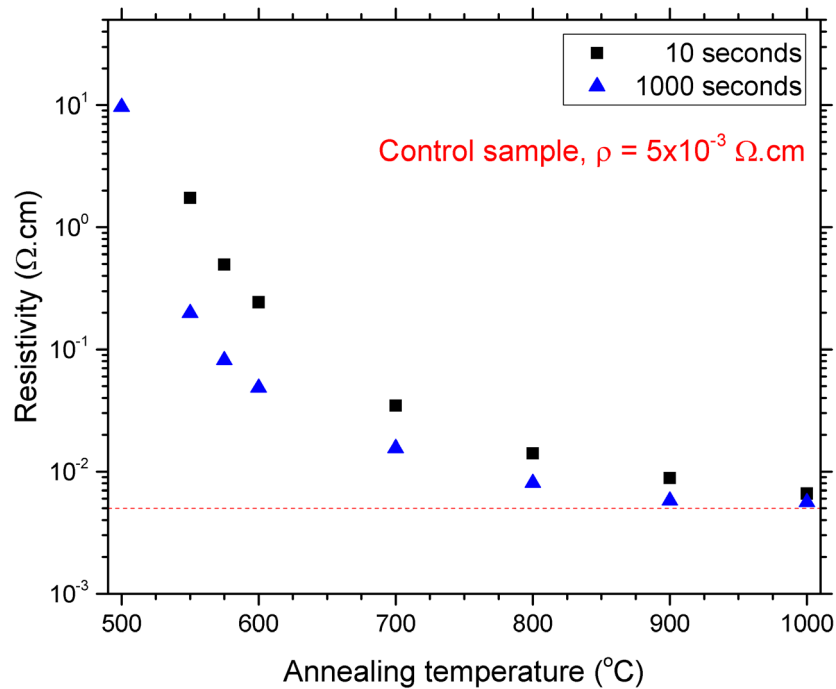


Figure 6.11 Resistivity as a function of RTA temperature and duration for p-type SOI samples ($1.8\mu\text{m Si}/1\mu\text{m SiO}_2/500\mu\text{m Si}$) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{ cm}^{-2}$.

6.9.2 n-type SOI samples

Figure 6.12 presents resistivity of n-type SOI samples following isochronal and isothermal annealing studies undertaken after high energy ion implantation. Isothermal annealing was undertaken at 600°C for durations of 3, 10, 100 and 1000 seconds. Resistivity following isochronal annealing with a duration of 10 seconds is shown for a range of temperatures between 600 and 1000°C. As was the case for p-type samples, characterisation of as-implanted n-type samples revealed undetectable levels of electrical conductivity and samples are not shown. For RTA temperatures $\geq 600^\circ\text{C}$, a strong temperature dependence is again shown, with samples displaying a rapid restoration of electrical properties as temperature is increased. Resistivity is measured at $\sim 2 \times 10^{-3} \text{ ohm.cm}$ following a 10s anneal at 600°C. A value only twice that of control samples. A strong dependence to annealing duration is also suggested. Samples annealed at 600°C for 1000s are found to display a level of electrical resistivity approaching half that of samples annealed at the same temperature for 10s. Resistivity values approaching $1.2 \times 10^{-3} \text{ ohm.cm}$ are measured, a level almost fully restored to that of control samples.

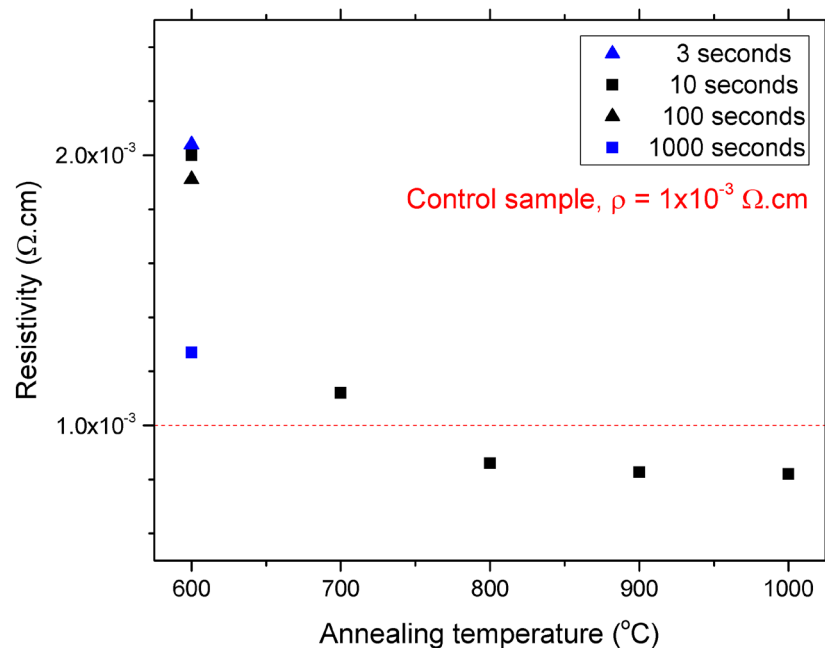


Figure 6.12 Resistivity as a function of RTA temperature and duration for n-type SOI samples ($1.9 \mu\text{m Si}/2 \mu\text{m SiO}_2/500 \mu\text{m Si}$) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{ cm}^{-2}$.

It can be noted that for annealing temperatures $\geq 800^\circ\text{C}$, resistivity values are found to be less than that of control samples. This is suggestive of an excess concentration of

un-activated dopant within the original SOI wafer that is later free to become activated during RTA. An explanation may be offered by considering complimentary research findings reported by Smith et al. The use of vacancy defect engineering for semiconductor applications achieved a comparable enhancement, increasing phosphorus activation for thin SOI substrates [167]. Here a mechanism was suggested whereby phosphorus-interstitial clustering was reduced as a result of vacancy-interstitial annihilation. Increased phosphorus activation over non vacancy engineered samples was found.

While general behaviour can be considered broadly similar for both n-type and p-type samples, it should be noted that reductions in resistivity are revealed to occur more rapidly in these n-type samples than is found for p-type samples shown in Figure 6.11. Concentrations of phosphorus are close to exceeding 10^{19} cm^{-3} , a level of solubility suggested possible in literature at temperatures of $\sim 600^\circ\text{C}$ for silicon [162, 166]. Such a temperature is considerably lower than the $\sim 900^\circ\text{C}$ required to achieve levels of boron solubility present in p-type samples. Results presented here can be considered in good agreement with these reported findings, remaining consistent with previously reported results for a proof of principle study where Bennett et al reported restoration of electrical properties in vacancy engineered silicon doped with phosphorus at a comparable 600°C [14].

The restoration of electrical resistivity at 600°C is found to occur more gradually for samples shown in Figure 6.12 than that reported in literature by Bennett et al. Nano-film samples of n-type with a device layer thickness of 100 nm were found to achieve almost complete recovery after 10s annealing at 600°C [14]. This behaviour is not matched in results presented here. Samples containing an identical phosphorous dopant investigated in this work can be seen to approach full recovery only after an annealing duration of 1000s at 600°C . RTA effects are widely studied, with effects on damage demonstrated to be generally temperature dependent but thickness independent [155]. As a result, this disparity is unlikely to be explainable simply due to the considerable changes in material thickness between experiments (100 nm to $1.9 \mu\text{m}$). An explanation may be found by considering however the possibility of slight differences in physical temperatures in each set of experiments - with samples of Bennett et al possessing the higher temperature. Such an explanation appears plausible given the different equipment used in each work. Differences in values of thermal conductivity as a function of RTA duration reported between these two sample sets (and highlighted in

Figure 6.6) would however suggest a lower relative RTA temperature for the 100 nm samples of Bennett et al. This apparent contradiction is however resolved by the hypothesis of a relationship between vacancy concentration and thermal conductivity restoration rate introduced in section 6.6 and further discussed in section 6.7. Under such a hypothesis, the greater vacancy concentration present in the 100 nm samples studied by Bennett et al could explain the slower rate of restoration for k noted for Bennett's samples allowing a difference in RTA temperature as a result of calibration differences to offer a possible explain the more rapid restoration of resistivity.

6.10 Rapid Evaluation Through Reductions in Term ρk

With evaluation of thermoelectric performance undertaken through the metric z , where $z = S^2/\rho k$, or zT where $zT = S^2T/\rho k$ it can be seen that for successful thermoelectric materials it is important that reductions in thermal conductivity are not achieved at the expense of a significantly degraded electronic transport. Both properties are shown to be strongly impacted by high energy implants, and each displays a strong annealing temperature dependency. Potential performance improvements offered by defect engineering may be rapidly assessed through comparative evaluation of the term ρk . Material with potential for increased thermoelectric performance identifiable by values of ρk smaller than that of control samples.

Samples doped with boron – representing p-type material – were noted to display a slow increase in thermal conductivity for RTA temperatures $\leq 800^\circ\text{C}$, followed by a rapid increase in k for higher temperatures. Electrical resistivity was found to require temperatures $\geq 900^\circ\text{C}$ for the restoration of values to levels approaching that of control samples. The effect of these behaviours can be seen in Table 6.2, where thermal conductivity, resistivity and the term ρk are given as a function of annealing temperature for a duration of 10s. With $\rho k = 7 \times 10^{-3} \text{ W}\Omega/\text{K}$ for control samples, potential improvements or reductions over that of control samples are also noted.

The high activation temperatures required for boron impurities in p-type crystalline silicon are shown to present challenges for this defect engineering approach. Restoration of electrical properties to levels in line with control samples occurs at temperatures significantly greater than those appropriate for sustaining the large reductions in thermal conductivity initially achieved following self- implantation. For samples annealed at 600°C , thermal conductivity is 9.4 W/mK , a 15x reduction over

values for control samples and bulk c-Si. Resistivity however is 243×10^{-3} ohm.cm. A value 48x larger than resistivity measured in control samples. As a result, evaluation of ρk suggests effects on thermoelectric performance will be detrimental, with ρk increased rather than reduced.

Table 6.2 Results of k , ρ , term ρk and reductions in term ρk over control samples as a function of annealing temperature with a duration of 10 seconds for p-type samples.

	RTA Temperature (°C)				
	600	700	800	900	1000
k (W/mK)	9.4	11.9	16.1	48.3	69
ρ (Ω .cm)	0.243	0.035	0.014	0.009	0.007
ρk (W Ω /K)	22.8×10^{-3}	4.2×10^{-3}	2.3×10^{-3}	4.3×10^{-3}	4.8×10^{-3}
Reduction in ρk over control	-	1.6x	3.0x	1.6x	1.5x

For samples annealed at 1000°C, thermal conductivity is shown to be 69 W/mK, a value only half that of control samples. Resistivity is however shown to be 7×10^{-3} ohm.cm. A value almost equal to that found in control samples where $\rho = 5 \times 10^{-3}$ ohm.cm. Evaluation of the term ρk for these samples reveals a 1.5x reduction over control samples suggesting a potential, albeit minor, improvement in thermoelectric performance. Comparable potential is suggested for samples annealed at temperatures of 700°C and 900°C. In the first case, reductions in thermal conductivity made possible through defect engineering are offset by increased levels of resistivity over that of control samples; in the second case reductions in electrical resistivity are partnered with a much increased thermal conductivity.

Comparative evaluation against control samples reveals a best result for p-type SOI samples annealed at 800°C. A 3 fold reduction in ρk for p-type SOI samples is achieved. Here a resistivity value ~ 3 x greater than that of control samples is achieved alongside an ~ 9 x reduction in thermal conductivity. While such results offer promise, they can be considered considerably poorer than the order of magnitude improvement in performance returned for defect engineered nano-film samples previously reported. By comparison, Bennett et al achieved a reduction in ρk over control samples of ~ 10 x by combining a 10 fold reduction in thermal conductivity with an almost completely restored electrical resistivity, albeit using n-type samples [14].

For results on n-type samples doped with phosphorus in this current study, thermal conductivity reveals significant reduction at 600°C before undergoing rapid restoration for RTA temperatures $\geq 700^\circ\text{C}$. Unlike p-type samples however, electrical resistivity is only modestly inferior to control samples at 600 °C; suggesting significant potential.

Results for n-type samples annealed for a duration of 10 seconds can be seen in Table 6.3, where thermal conductivity, resistivity and the term ρk are shown as a function of annealing temperature between 600°C and 1000°C. With n-type samples yielding $\rho k = 1.4 \times 10^{-3} \text{ W}\Omega/\text{K}$, a comparative evaluation of improvement over control samples is also presented.

For all samples, evaluation of ρk is shown to reveal reductions over control samples – albeit modest in the case of samples subjected to RTA at higher temperatures. At 900°C and 1000°C almost no reduction in thermal conductivity is found and reductions in ρk are driven by levels of resistivity below that of control samples. Samples annealed at temperatures of 700°C and 800°C suggest potential improvements in thermoelectric performance by a factor of ~ 2 . In each case significant restoration of electrical conductivity is noted, however annealing temperatures produce a thermal conductivity more than an order or magnitude greater than found in as-implanted material.

The greatest potential is identified in n-type samples annealed at temperatures of 600°C. A rapid restoration of electrical conductivity - with samples only half that of control samples - is combined with significantly reduced levels of thermal conductivity. For these samples $\rho k = 2.3 \times 10^{-4} \text{ W}\Omega/\text{K}$, a reduction by a factor of 6 over control samples.

Table 6.3 Results of k , ρ , term ρk and potential improvement/reductions in thermoelectric performance over control samples as a function of annealing temperature with a duration of 10 seconds for n-type samples.

	RTA Temperature ($^\circ\text{C}$)				
	600	700	800	900	1000
k (W/mK)	11.7	58.8	87.8	129.8	140
ρ ($\Omega\cdot\text{cm}$)	0.0020	0.0011	0.00086	0.00083	0.00082
ρk (W Ω /K)	2.3×10^{-4}	6.5×10^{-4}	7.6×10^{-4}	1.1×10^{-3}	1.2×10^{-3}
Reduction in ρk over control	6.1x	2.2x	1.8x	1.3x	1.2x

It can be noted that Figure 6.9 reveals significant sensitivity in thermal conductivity to RTA duration at 600 °C, even for short duration RTA's. For example thermal conductivity after a 10s anneal can be seen to be 1.7x greater than for samples annealed for only 3s. Further evaluation focussed on n-type SOI samples annealed at 600°C is shown in Figure 6.13, where thermal conductivity and resistivity as a function of annealing durations (3-1000s) are presented for n-type samples included in Experiment I. Figure 6.13 also identifies corresponding reductions in ρk for each sample.

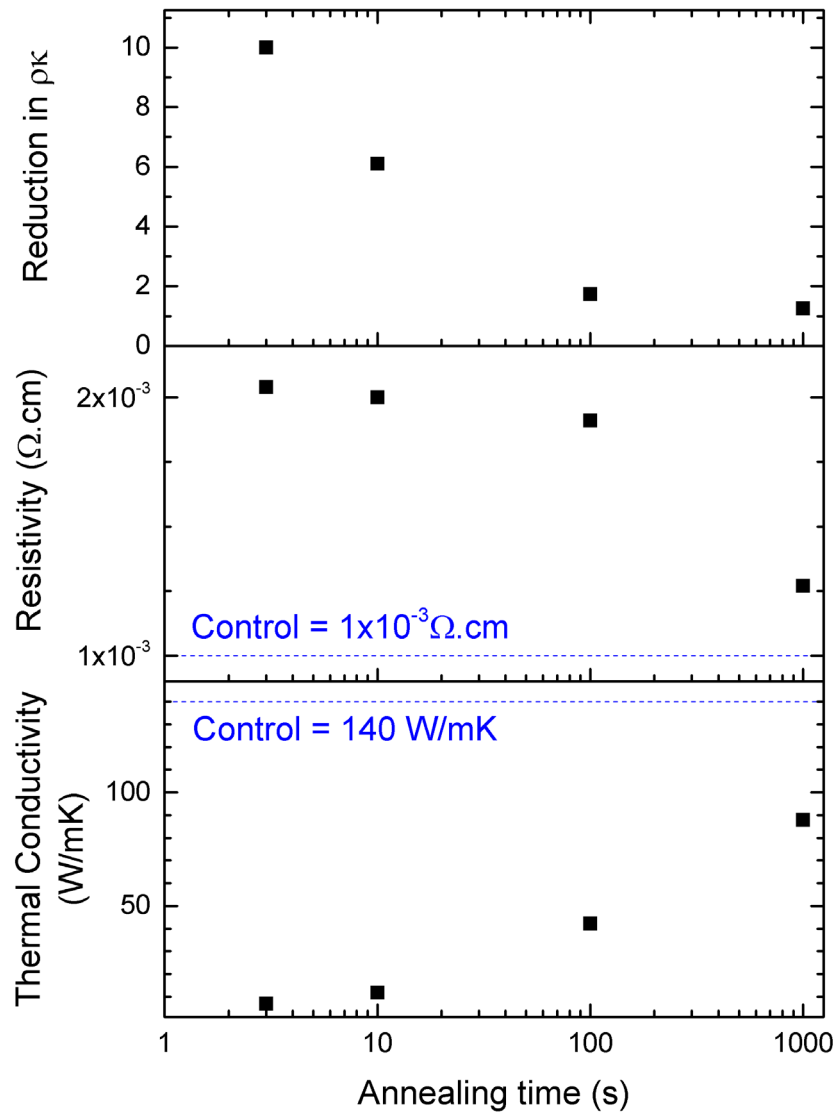


Figure 6.13 Thermal conductivity and Resistivity as a function of RTA duration at 600°C for n-type SOI samples ($1.9\mu\text{m Si}/2\mu\text{m SiO}_2/500\mu\text{m Si}$) following self-implantation with a high energy ion beam combining a beam energy of 2 MeV and a fluence of $8 \times 10^{15} \text{cm}^{-2}$. Also shown is reduction in term ρk over that of control sample.

A trend of increasing thermal conductivity and decreasing resistivity as a function of increasing RTA duration is clearly shown, while greatest reductions in ρk are shown to

occur at short RTA durations. Best results are achieved for n-type samples annealed at 600°C for 3s. Thermal conductivity is 6.9 W/mK- a 20 fold reduction over that found in as-implanted samples. Resistivity is measured as 2.04×10^{-3} ohm.cm – twice that of control samples. These results return a value of $\rho k = 1.4 \times 10^{-4}$ W Ω /K demonstrating a 10x improvement over control samples; a further increase over results in Table 6.3. Such a value is in excellent agreement with the previous study by Bennett et al. Defect engineering was applied to similarly phosphorus doped silicon with a reduced device layer thickness of 100nm and ρk found to reduce by a comparable factor of ~ 10 [14].

To summarise; for samples engineered with vacancy type defects, evaluation of the term ρk provides a straightforward and rapid means by which to jointly evaluate properties of electrical resistivity and thermal conductivity. Where thermoelectric materials are typically compared using zT or z , reductions in ρk can be considered indicative of potential increases in these metrics. Investigation of n-type and p-type SOI samples reveal both components of ρk are significantly impacted by high energy implant. Restoration of both ρ and k is strongly dependent upon annealing temperature and duration. Challenges in minimising ρk presented by p-type SOI samples are readily identified. Significant reductions in thermal conductivity are achievable, but the high temperatures required for restoration of electrical conductivity limit leveraging of this success. Best results for boron doped samples are found at 800°C where ρk is shown to be reduced by a factor of 3. A value lower than the order of magnitude reduction expected. For n-type SOI material, temperatures required for restoration of electrical conductivity are shown to be significantly lower than for boron doped p-type material. Significant reductions in k are well aligned with rapid restoration in ρ . Best results are obtained for samples annealed for 3 seconds at 600°C. Thermal conductivity is shown to remain greatly reduced, with $k = 6.9$ W/mK for an SOI device layer of $1.9 \mu\text{m}$ thickness. Control sample thermal conductivity was 140 W/mK. Resistivity is twice that of control samples and ρk is reduced by a factor of 10. Such reductions match the best reductions reported by Bennett et al on n-type SOI with a considerably thinner 100 nm thick device layer [14].

6.11 Seebeck Coefficient

Room temperature Seebeck coefficient measurements were undertaken for vacancy engineered samples subjected to a 3s duration RTA at a temperature of 600°C, applying a U_1 vs U_2 approach presented by de Boer [110] and discussed in Chapter 3.

Figure 6.14 presents a plot of recorded voltage data between temperatures of 301K and 299K revealing the strongly linear relationship between recorded voltages. A linear fit to these data can be seen in red. An R square value for this fit is returned of 0.999.

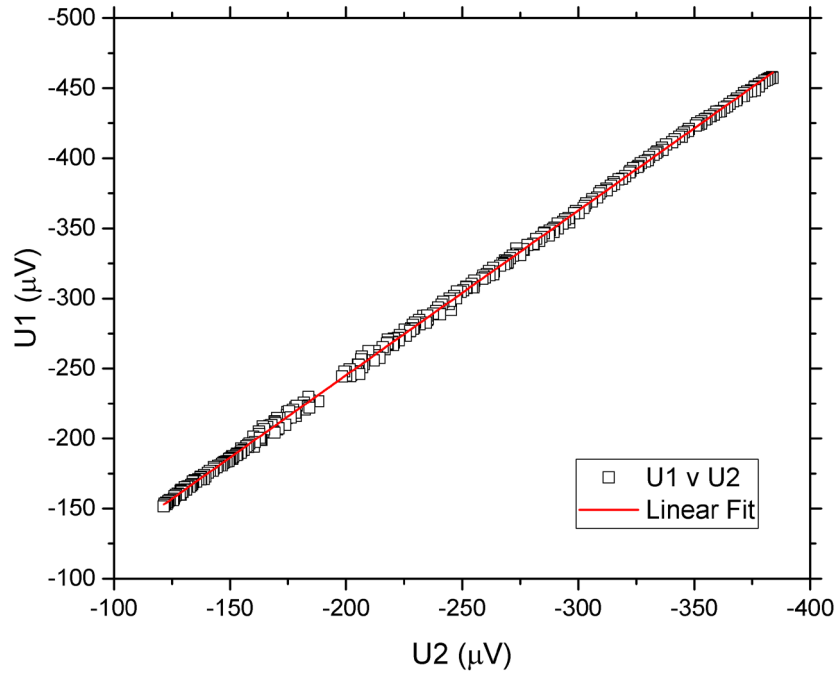


Figure 6.14 Plot of U_1 vs U_2 recorded for the determination of room temperature Seebeck coefficient on an n-type sample subjected to vacancy engineering followed by an RTA of 600°C for 3 seconds duration. A linear fit to this data can be seen in red, with the slope of this line used for the calculation of Seebeck coefficient using an approach comparable with that presented by de Boor [110].

Seebeck coefficient at $\bar{T} = 300\text{K}$ for this sample can be given as $-246.6 \mu\text{V/K}$, derived from a slope of 1.175 obtained from the linear fit shown in Figure 6.14. Such a value is slightly greater than that of control samples, $S \sim -235 \mu\text{V/K}$ - explainable by a slightly increased electrical resistivity – and remains in line with both values and trends of Seebeck coefficient for bulk silicon as a function of carrier concentration reported in literature [10, 168].

Results of corresponding measurements for vacancy engineered n-type SOI samples as a function of RTA duration at a temperature of 600°C are shown in Figure 6.15. Values of Seebeck coefficient are shown to reduce as RTA duration is extended. A finding in line with expectations given the improving nature of electrical conductivity found in such samples and presented in Figure 6.13.

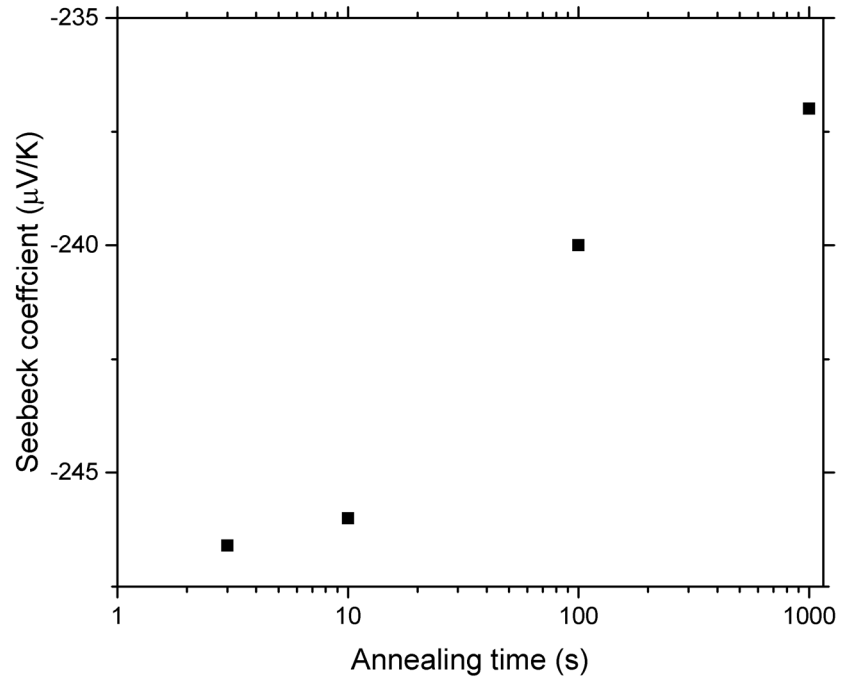


Figure 6.15 Room temperature Seebeck coefficient as a function of annealing duration at 600°C for n-type SOI samples subjected to vacancy engineering.

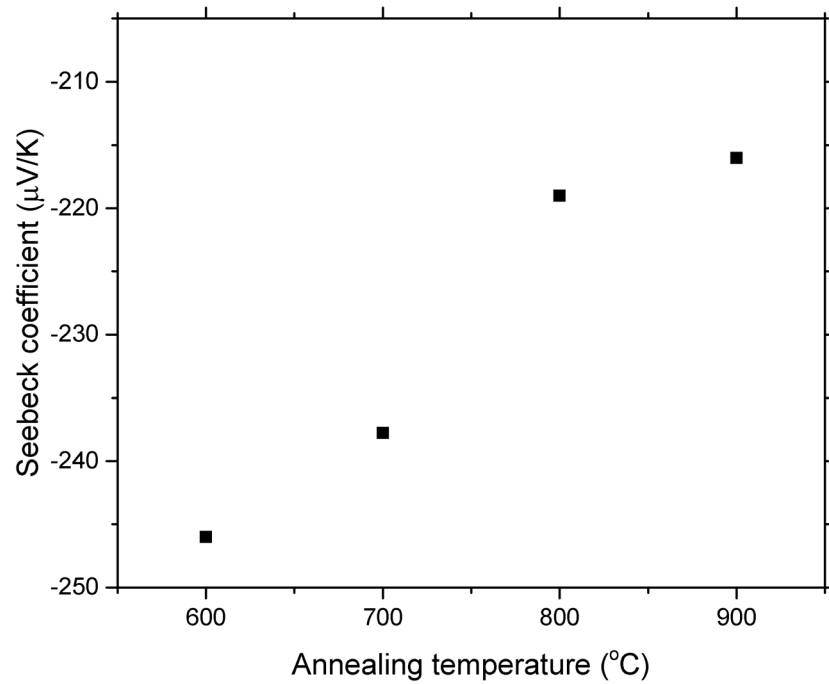


Figure 6.16 Room temperature Seebeck coefficient as a function of annealing temperature for n-type SOI samples subjected to vacancy engineering.

A similar behaviour is noted for Seebeck coefficient as a function of annealing temperature. Results for RTA's with a duration of 10s are shown in Figure 6.16. Seebeck coefficient is again found to decrease as RTA temperature is increased towards

1000°C. Such behaviour is in line with the strong dependency of electrical conductivity restoration on RTA temperature presented for these samples in Figure 6.12.

6.12 Thermoelectric Performance

Thermoelectric performance of these best result samples - n-type, 600°C RTA – can be evaluated through calculation of the term z , where $z = S^2/\rho k$. The use of such an approach removes the limitation offered through zT where values calculated are a direct product of temperature.

Room temperature z for these n-type SOI samples is shown in Figure 6.17. Comparison of Figure 6.13 showing reduction in ρk as a function of RTA duration at 600°C and that of z given in Figure 6.17 reveal close similarities, demonstrating the value in ρk evaluation as a means of rapid identification of samples with greatest thermoelectric potential.

A best value of $z = 4.4 \times 10^{-4} \text{ K}^{-1}$ is returned for samples annealed for a duration of 3 seconds. Such a result reveals a significant improvement over the same term in bulk c-Si as a result of increased phonon scattering and reduced phonon mean free path achieved via the introduction of large concentrations of vacancy defects. Benchmark values for thermoelectric performance in bulk single crystalline silicon are typically taken from findings presented by Weber & Gmelin. Transport properties were investigated between temperatures of 2 and 300K, with findings allowing approximation of the now well established room temperature figure-of-merit of $zT = 0.01$ [63]. Re-evaluation of results of Weber & Gmelin allows a similar approximation for z at 300K to be made. Bulk c-Si is found with $z = 3.15 \times 10^{-5} \text{ K}^{-1}$. Best results on these defect engineering thin-film samples demonstrate a factor of 14 increase over this bulk c-Si value. Such an increase is significant when considering the defect engineered samples have no nanodependence.

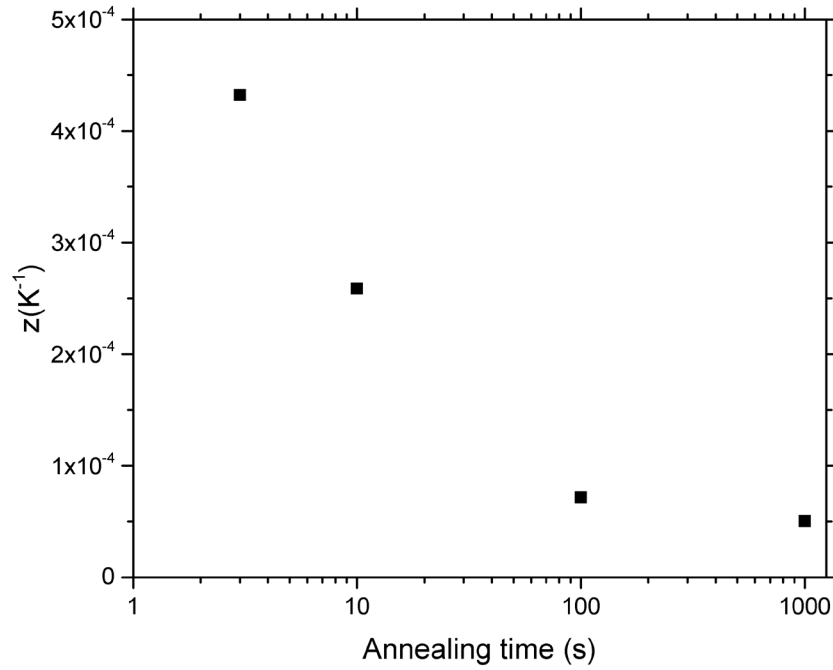


Figure 6.17 Room temperature thermoelectric factor z as a function of annealing duration for temperatures of 600°C for n-type SOI samples following vacancy engineering.

An evaluation of z can be similarly undertaken for other thermoelectric materials, allowing direct comparison with defect engineered material prepared in this work. Such an evaluation is presented in Figure 6.18 where extracted values for z are shown. Values for bulk c-Si and commercial Bi_2Te_3 are shown alongside high zT CuSe bulk and ultra high zT SnSe. Also included are values for alternative approaches for thermoelectrics using silicon.

Results presented in Figure 6.18 offer some interesting insights. Bi_2Te_3 , a material currently favoured for commercial application demonstrates greatest thermoelectric performance of all materials included. High figure-of-merit SnSe bulk, with a famously reported $zT = 2.6$ is shown to offer only a comparable z value. The large figure-of-merit reported shown to be a direct result of their use of a larger \bar{T} value in its calculation. Reported temperature is ~ 2.6 times larger than the 350K used by Bi_2Te_3 with $zT = 1$. The same is true for bulk CuSe ($zT = 1.8$) where z is shown to be slightly lower than for Bi_2Te_3 .

Of greater interest is the relative performances indicated for silicon thermoelectric approaches. Silicon nanowires featuring surface roughness, “holey” silicon nanomembranes and high power factor polycrystalline nanofilms are all shown to offer levels of thermoelectric performance significantly greater than that offered by bulk c-Si.

In all cases, values for z approach that of Bi_2Te_3 and demonstrate the distinct advantages to silicon thermoelectrics offered by nanoscale effects. Requirements for nanoscale dimensions to achieve performance are however a feature for these materials, presenting challenges for direct device application. Nanocrystalline silicon with bulk material dimensions - and thus a removal of dimensional nanodependence - reported by Bux et al is shown to offer only a marginal improvement over that of bulk c-Si.

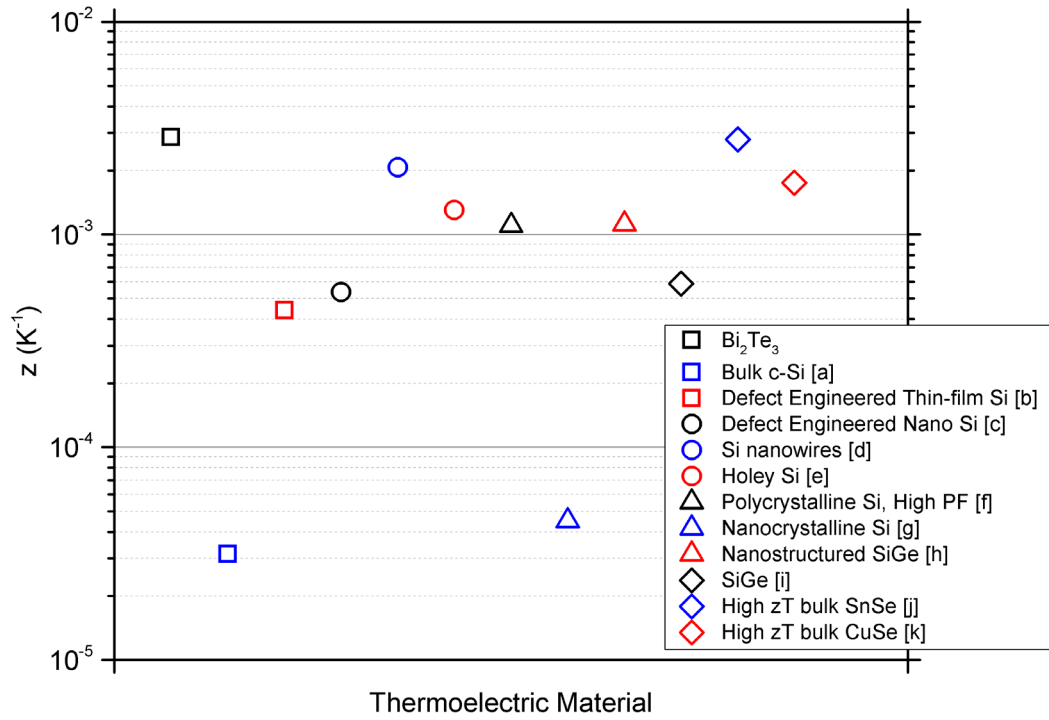


Figure 6.18 Values of z , where $z = S^2/\rho k$ for a range of thermoelectric materials, allowing direct comparison of thermoelectric performance to be made. The value for Bi_2Te_3 at 350K, a material currently favoured in commercial application is shown alongside **a)** bulk c-Si at 300K [63], **b)** defect engineered thin film c-Si at 300K (this work), **c)** defect engineered nanofilm c-Si at 300K [14], **d)** Rough silicon nanowires at 300K [8], **e)** nanoporous silicon nanomembrane at 300K [69], **f)** high power factor polycrystalline silicon nanofilm at 300K [25], **g)** nanocrystalline bulk silicon at 300K [70], **h)** nanostructured bulk SiGe at 850K [49], **i)** bulk SiGe at 850K [49], **j)** high zT SnSe bulk at 923K [46], **k)** high zT CuSe bulk at 973K.[45]

Best values obtained on thin film c-Si using defect engineering presented in this work achieve values of z in line with those obtained on defect engineered nano-film c-Si by Bennett et al [14]. Values in both cases are considerably increased over that of bulk c-Si and are shown to be only a factor of 2 away from the 10^{-3} K^{-1} magnitude demonstrated by alternative high performance materials shown. This improvement is shown to produce results comparable with SiGe, a material with a history of application

at $>800\text{K}$ and suggests a promising future for thermoelectric applications when considering the broader advantages offered by silicon as a material.

That comparable reductions in thermal conductivity were also found in free standing c-Si films with thicknesses of $2\text{ }\mu\text{m}$ suggest that equivalent improvements in z can also be expected in this free standing material providing appropriate doping concentrations are added. Such material offers significant practical utility in thermoelectric devices.

It can be noted that z would have reached $\sim 9 \times 10^{-4}\text{ K}^{-1}$ had full restoration of electrical resistivity been achieved with a 3s RTA duration. The effect hypothesised previously, whereby larger concentrations of vacancies in as-implanted material appear to act to delay restoration of k offers promise in this respect. Extending the RTA duration even to 10s without penalty on thermal conductivity would enable such a level of thermoelectric performance to be achieved.

Chapter 7: Conclusions and Further Work

7.1 Conclusions

The development of next generation “high performance” thermoelectric materials must balance competing definitions of the term “performance”. Good thermoelectric properties required for efficient thermal-electrical power conversion should also meet expectations around earth abundance and non-toxicity – both properties lacking in current generation commercial materials. Materials must also remain aligned to manufacturing capabilities if promise offered by fundamental research is to be translated into device application.

Silicon offers significant advantages in many of these areas. It benefits from considerable manufacturing know-how and capability through extensive use in semiconductors, while it meets requirements for both earth abundance and non-toxicity. As a thermoelectric material, highly doped silicon has demonstrated the high PF required for maximising power generation. However its efficiency, along with its ability to maintain the temperature gradient required for power conversion is significantly impacted by high levels of thermal conductivity. Research in the area of silicon thermoelectrics has been typified by a focus on addressing this challenge. Where approaches have started with high PF silicon and sought to reduce thermal conductivity, opportunities have arisen through targeted reductions in phonon mean free path. Historically, rough nanowires and porous nanomembranes have been highly effective in introducing phonon scattering and reducing thermal conductivity. These approaches are however highly dependent on the use of nanoscale dimensional material, presenting obvious challenges for translation to devices.

While metamaterials offer a possible solution to nanodependence, particularly for nanowires where complex arrays have been developed to produce larger scale samples, theoretical predictions suggested that an alternative approach may be possible through the introduction of large concentrations of vacancy defects to bulk c-Si if a means of introduction could be found. Such a concept was previously demonstrated on nano-film c-Si using high energy ion implantation. It was theorised that large concentrations of vacancies were created during self-implantation, producing significant phonon scattering and offering explanation for the large reduction in thermal conductivity noted. The potential for this approach to be scalable to materials with microscopic dimensions was suggested.

This thesis has investigated the scale up of vacancy defect engineering; targeting the creation of vacancy defect concentrations in thin-film c-Si using high energy implantation to reduce thermal conductivity and improve thermoelectric performance. Material containing both n-type and p-type dopants prevalent in thermoelectric applications were investigated. A modified version of this defect engineering method was also developed, allowing application of this approach to free standing c-Si materials and the removal of a requirement for a layer of isolating buried oxide. The main conclusions can be listed as follows:

- The introduction of vacancy defects in c-Si materials with thicknesses up to $2\text{ }\mu\text{m}$ have been shown to significantly reduce thermal conductivity. Such thicknesses are more than an order of magnitude greater than previously reported demonstrating *i)* that scaling of this approach to thin films materials with thicknesses $> 1\text{ }\mu\text{m}$ is equally as effective at reducing thermal conductivity, and *ii)* that the low levels of thermal conductivity previously possible are not nanodependent.
- Vacancy concentrations have been identified in defect engineered c-Si using positron annihilation spectroscopy, confirming their presence in material with a reduced thermal conductivity and theoretical predictions about their effects on phonon scattering.
- A method of producing vacancy rich material without a requirement for an isolating layer of buried oxide layer is shown to be successful. Reductions in thermal conductivity for free standing material are found to be equal to that shown possible in SOI device layers.
- Reductions in thermal conductivity are shown to be independent of impurity type. Thermal conductivity is reduced to the same value for n-type, p-type and dopant free silicon.
- A significant difference in thermoelectric performance is noted between p-type and n-type defect engineered material. The higher annealing temperature required for dopant activation with boron presents challenges in maintaining the large reductions in thermal conductivity identified in as-implanted samples. Best results on p-type material are shown to be 3x greater than control samples.

- Best results demonstrate an improvement in thermoelectric performance of defect engineered n-type thin-film c-Si by a factor of 10 over that found in control samples, and a factor of 14 over benchmark bulk c-Si.

The main objectives of this work were identified as the *demonstration of upscaling of the vacancy defect engineering technique*, and the *development of an approach allowing free standing defect engineered silicon to be produced without a requirement for an isolating layer of buried oxide layer*. The following sections discuss the main conclusions in the context of these objectives whilst bringing together additional findings of interest. A third objective to *develop a means of obtaining thermal conductivity measurements on defect engineered samples* was also identified. The reporting of this work has already proven of benefit to researchers seeking to undertake thermal conductivity measurements and application was used for measurement of samples discussed in Chapter 6. Discussion around this approach and its conclusions is contained within Chapter 4 which is dedicated wholly to its development and suitability for purpose.

7.1.1 *Scaling of defect engineering to c-Si thicknesses > 1 μ m*

Experiment I and II both allowed the investigation of upscaling, introducing vacancy defect concentrations to thin-film thickness c-Si for the purpose of reducing thermal conductivity. Materials up to 2 μ m thick were investigated, offering increases in thickness more than an order of magnitude greater than previously reported. While Experiment I utilised SOI material using a buried oxide layer to act as an isolating region and prevent interregional mixing of vacancy and silicon interstitial, Experiment II developed a modified approach allowing application on free-standing thin film c-Si. Using this approach the majority of silicon interstitials were predicted by TCAD simulation to be ejected from the rear surface of this material during self-implantation, removing any requirement for an additional isolating layer. Significant reductions in thermal conductivity were found for both experiments demonstrating the effectiveness of vacancy defect engineering to be scaled to considerably thicker material. Importantly, application to free standing thin-films was shown to produce material with equally reduced thermal conductivity.

Values of room temperature thermal conductivity in as-implanted samples obtained during Experiment I and Experiment II were highly convergent, despite significant variation in k for control samples. These results suggest that a minimum value for

thermal conductivity using vacancy defect concentrations may approach $k = 4 \text{ W/mK}$, implying that maximum reductions may have an absolute limit rather than being proportional to initial value.

With reductions in thermal conductivity shown to scale successfully, this method for reducing thermal conductivity can be considered limited only by available beam energy. TCAD simulation of a 30 MeV implant into bulk c-Si with a thickness of $10 \mu\text{m}$ is shown in Figure 7.1. With vacancy defect concentrations shown in black, and concentrations of silicon interstitials shown in red, it can be seen that under such conditions it could be possible to produce net vacancy defects across the entire sample.

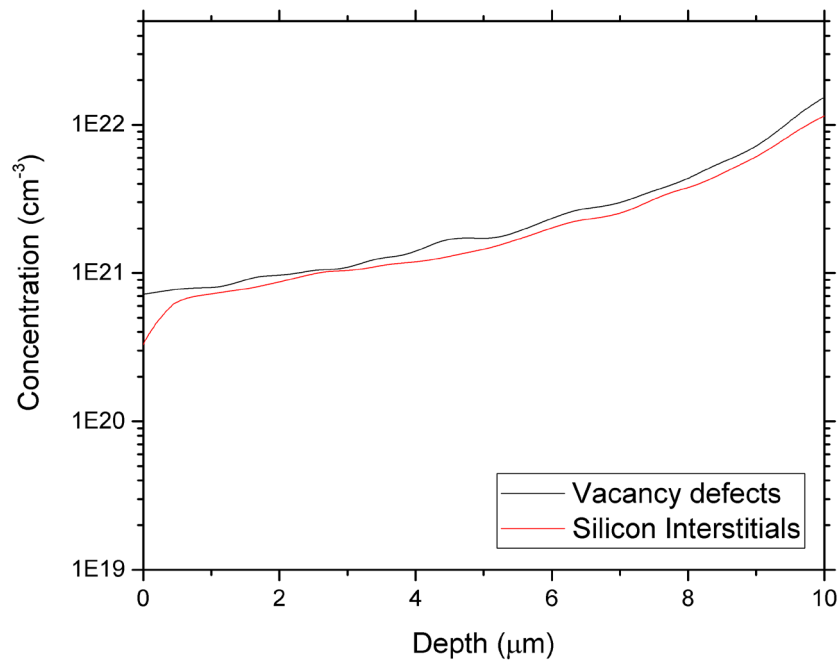


Figure 7.1 TCAD simulation results for a 30 MeV implant into $10 \mu\text{m}$ thick c-Si. Concentrations of vacancy defects and silicon interstitials created are shown, revealing a net concentration of vacancy defects throughout the entire sample.

7.1.2 Influence of vacancy concentration on thermal conductivity

TCAD simulations predicted net vacancy concentrations of 8-9% in SOI material produced during Experiment I, and $\sim 4\%$ in free standing thin-film material produced during Experiment II. Values of room temperature thermal conductivity in as-implanted samples were nonetheless found to be highly convergent. The restoration of k in response to annealing was found to be strongly dependent on annealing temperature and duration, however the rates with which restoration took place were significantly different. SOI samples were found to restore more slowly than for thin-film samples.

While control sample k was lower in free standing samples, these results nonetheless introduce the possibility of an interesting hypothesis. Namely that a threshold for vacancy concentrations exists where lowest thermal conductivity occurs. Increasing vacancy concentrations beyond this threshold has limited impact with respect to further reductions. But these larger vacancy concentrations may yet act to slow the rate with which thermal conductivity is found to restore during annealing. This hypothesis has some basis in theory however the implications of k as a function of vacancy concentration together with k as a function of cluster size at a given concentration were not fully explored. Such a hypothesis may offer significant value by allowing an increase in RTA duration before significant increases in thermal conductivity are detected.

7.1.3 *Influence of dopant type*

The use of boron and phosphorus doped SOI in Experiment I and dopant free c-Si in Experiment II allowed the effects of dopant on results to be evaluated. For thermal conductivity reductions, results were found to be insensitive to impurity and achievable reductions in k were found to be directly comparable for all samples studied. This is in line with expectations given the low concentrations of impurities present however such findings offer important confirmation. The application of defect engineering for reduced thermal conductivity is applied to boron doped and undoped silicon for the first time in this work.

Dopant type was shown to be highly influential in the restoration of electrical properties during post implant annealing. The restoration of electrical properties to levels in line with control samples required significantly greater temperatures for boron than for phosphorus. These higher temperatures presented challenges for boron doped samples when seeking to preserve large reductions in thermal conductivity while simultaneously restoring electrical properties following as-implanted values. As a result, maximum increases in thermoelectric performance were significantly restricted in p-type samples. An increase of 3x was noted over vacancy free control samples. Such challenges were not present in phosphorus doped samples. The reduction of resistivity to levels in line with that of control samples was possible with only small increases in thermal conductivity. Best results identified improvements in thermoelectric performance by a factor of 10 over control samples.

7.1.4 *Increased thermoelectric performance*

Evaluation of thermoelectric performance using the term z revealed interesting outcomes. Bismuth Telluride was shown to be the best performing material amongst those evaluated, despite materials also evaluated reporting record high values of figure-of-merit. Best results for defect engineered c-Si produced by this study - obtained following a 3s 600°C RTA - revealed a value of z that was 10 times greater than that of control samples, and 14 times greater than that of benchmark bulk c-Si. This increased z value was comparable with that of SiGe and only a factor of 2 away from approaching the same order of magnitude as bismuth telluride. That this is possible in thin-film c-Si material with no nanodependence and that is visually indistinguishable from defect free bulk c-Si offers significant promise.

It can be noted however that such performance was achieved only on n-type material. Material doped with boron was unable to achieve more than a 3 fold increase in performance. These results present challenges for conventional thermoelectric device architectures which rely of both n-type and p-type material.

A solution can be had by considering application of this best performing n-type c-Si to a thermoelectric device using a novel unipolar configuration.

Comsol simulation of a simple unipolar microharvesting thermoelectric generator using n-type material produced in this work can be seen in Figures 7.2 and 7.3. The thermoelectric device is configured in a planar architecture and features 12 legs of n-type defect engineered single crystalline silicon with electrical characteristics and a value of thermal conductivity as per best results. Installation is shown on top of a square heat source with a temperature of 315K. Surface temperatures resulting from heat flow are detailed in Figure 7.2, with flow shown to take place from the heat source to the square outer frame of the device before flowing equally through each of the 12 thermoelectric legs to a central air cooled hub at 300K.

Voltage produced as a result of this temperature gradient in the thermoelectric legs can be seen in Figure 7.3. With the darkest red identifying ground, a voltage potential of 25 mV is revealed between this point and the end of the circuit. While design and simulation are highly simplified, they nonetheless identify the opportunity offered by unipolar based thermoelectrics to allow effective utilisation of defect engineered silicon where only an n-type material is available.

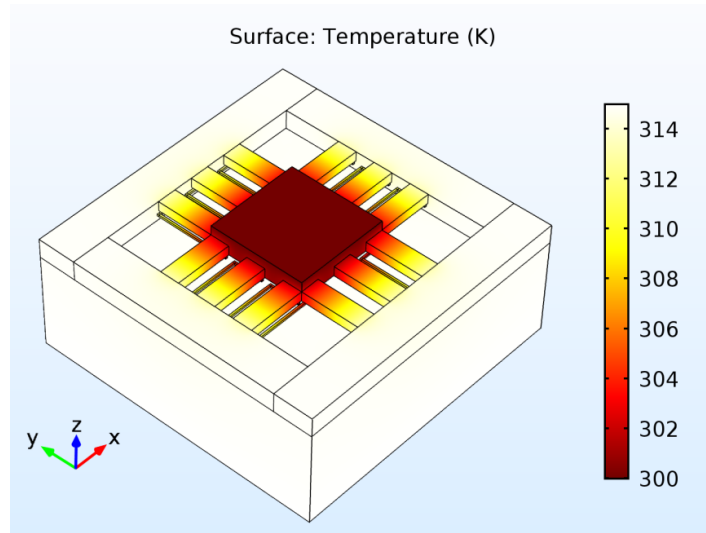


Figure 2. Comsol simulation of surface temperatures on a unipolar thermoelectric generator containing 12 thermoelectric legs on n-type defect engineered c-Si with properties identified in best samples from this work. The thermoelectric generator is shown mounted on a square shaped heat source at 315K.

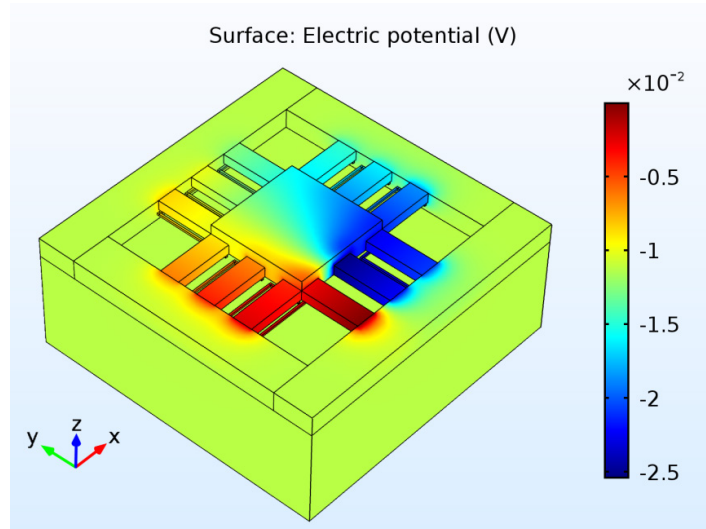


Figure 3. Comsol simulation of voltage potential on a unipolar thermoelectric generator containing 12 thermoelectric legs on n-type defect engineered c-Si with properties identified in best samples from this work.

7.2 Further work

This work has identified a number of important findings in the field of thermoelectrics, with conference presentation, workshop participation and peer reviewed publications ensuring dissemination of results to the wider research community. As typically found, the conclusion of this work offers the starting point of many new questions rather than a

final word. The most interesting are offered here in the hope that this work continues to stimulate conversation.

7.2.1 *Quantification of vacancy concentrations*

A significant limitation of the VEPAS study was that it was not possible to investigate the number of vacancies present under the scope of the original study. Such analysis is however possible and now offers significant value. Quantifying initial concentrations of vacancy defects and understanding changes in concentration during RTA may prove useful. Especially when viewed against changing properties of thermal conductivity as a function of annealing time. At the commencement of the project, the value of such analysis appeared greatest in allowing validation of TCAD simulation. This would indirectly allow implant optimisation and the minimisation of beam line run hours. Given the hypothesis that a threshold concentration may exist where minimum k is achieved, but that excess vacancies beyond this threshold may help slow the restoration of thermal conductivity there is now a broader opportunity offered through such a study.

7.2.2 *Testing the hypothesis of vacancy concentration versus k restoration*

The idea that increased vacancy concentrations may be unable to produce additional reductions in thermal conductivity but yet slow the restoration of thermal conductivity during RTA is an intriguing one. There is significant value to be had in testing this hypothesis and determining firstly whether it is valid, and secondly how significant any impacts are. Best results were achieved with samples that had experienced a slight increase in thermal conductivity relative to that found in as-implanted samples, and which displayed resistivity values not quite fully restored. The ability to delay even slightly the increase in thermal conductivity experienced during RTA may prove sufficient to allow full optimisation of results.

7.2.3 *Stability testing*

Previously reported stability tests on defect engineered c-Si suggested good stability of the low thermal conductivity achieved during long term exposure at 150°C, while stability for temperatures $> 600^\circ\text{C}$ is discussed during this work. The success of upscaling to materials $> 1\ \mu\text{m}$ brings closer the translation of this material to devices. There is considerable value to be had in now undertaking a stability test in a manner that is more representative of application environment; and in extending this test into the $150^\circ\text{C} < T < 600^\circ\text{C}$ range. Identification of the upper limits of working temperature

for these defect engineered materials may offer potential for use in additional applications with temperature environments $>150^{\circ}\text{C}$. Combining thermal cycling and mechanical vibration while studying effects on performance, and in particular sustainability of reductions in thermal conductivity will be important in establishing long term operational stability and operating temperature limits; both crucial for ensuring application opportunities.

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